FUSB3317

FUSB3317 is a highly integrated USB Power Delivery (PD) power Source controller for USB−C that implements all functionality of USB Power Delivery 3.1 (PD) and Type−C™ 2.0 including Programmable Power Supplies (PPS). The FUSB3317 directly interfaces with a DC−DC regulator saving the cost of a load switch FET.

FUSB3317 supports various protections, adaptive Under Voltage Protection (UVP), adaptive Over Voltage Protection (OVP), Over Current Protection (OCP), CC1 and CC2 Over Voltage Protection (CC_OVP), D+ and D− Over Voltage Protection (D_OVP), VCONN Over Current Protection (VCONN_OCP), and internal and external Over Temperature protection (I_TOP and E_OTP).

Features

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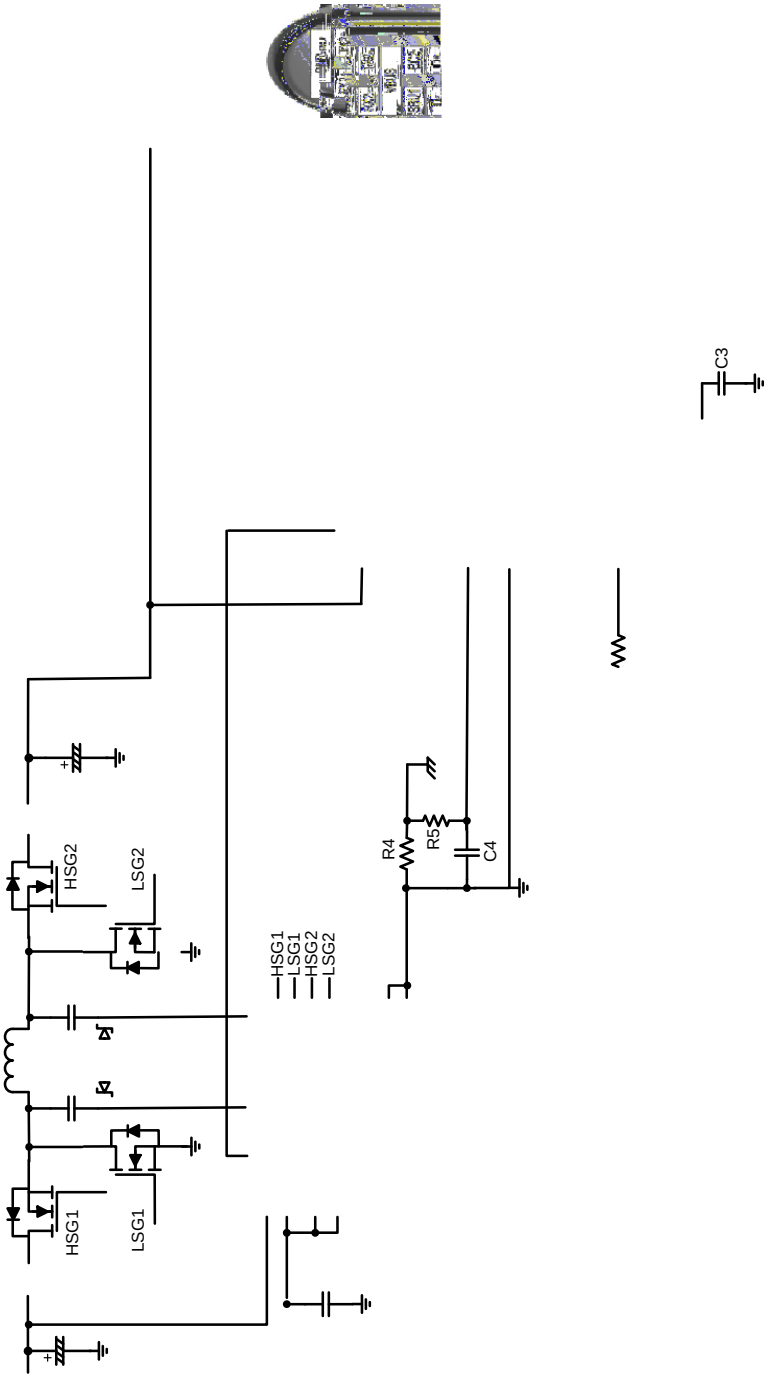


Figure 1. Application Schematic – Automotive DC/DC Reference Design Example

Block Diagram

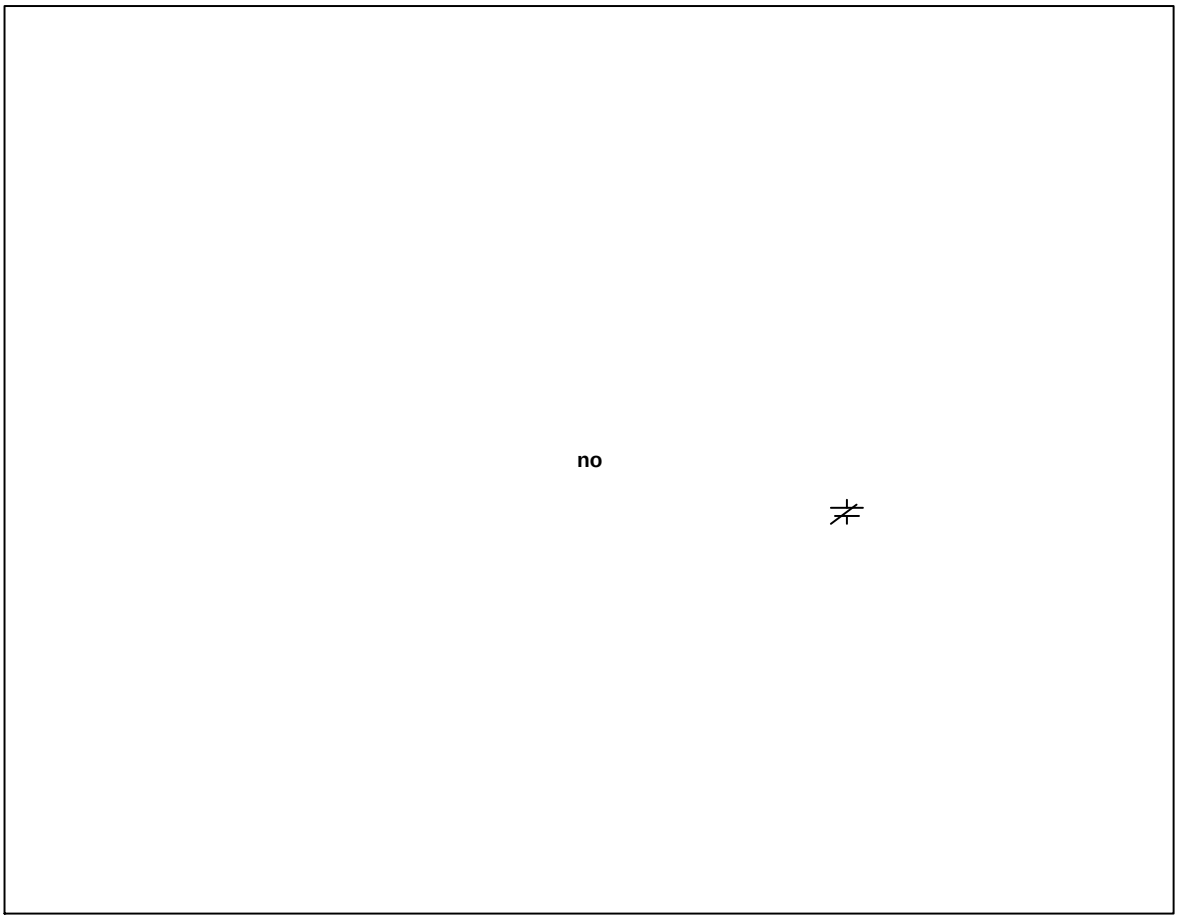


Figure 2. Simplified Block Diagram

PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	I/O Type	Description
11	VBUS	Input	Output VBUS voltage to the Type C connector (Input voltage to the FUSB3317 to check for OVP and UVP)
2	VBAT	Supply	Input power for the FUSB3317 directly from a battery for automotive applications or from a DC−DC supply for industrial
19	VDD	Output	Supply voltage generated internally from VBAT (output from FUSB3317). This pin is connected to a 1 μF external capacitor.
13	GND	Ground	Connect to board ground but not connector ground
12	CATH(FB)	Open Drain Output	Feedback to control the power supply. Typically connected to the error amplifier output of a DC−

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
VBAT Battery Pin Voltage (Note 1)	$V_{VBATMAX}$	−0.3 to 54	V
Connector Pins Voltage: VBUS, DISC, CATH, CC1, CC2, D+ and D−	$V_{HIGHMAX}$	−0.3 to 27 V	V
Low Voltage Pins: DC_EN, DON, IS−, VFB, IFG, BATUV, NTC, PDIV1 and PDIV0	V_{LOWMAX}	−0.3 to 6 V	V
Supply Output Range on Pin VDD	V_{VDDMAX}	−0.3 to 6 V	V
Current Sense Input on Pin IS+	V_{IS+MAX}	IS− + 0.1	V
Maximum Junction Temperature	$T_{J(max)}$	150	°C
Storage Temperature Range	T_{STG}	−65 to 150	°C
ESD Capability, Human Body Model (Note 2)	ESD_{HBM}	2	kV
ESD Capability, Charged Device Model (Note 2)	ESD_{CDM}	750	V
Lead Temperature Soldering Reflow (SMD Styles Only), Pb−Free Versions (Note 3)	T_{SLD}	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114)
   ESD Charged Device Model tested per AEC−Q100−011 (EIA/JESD22−

ELECTRICAL CHARACTERISTICS (continued)
For typical values, V_{VVBAT} = 12 V and T_A = 25°C. For min/max values, V_{VVBAT} = 5.5 V to 36 V and T_J = −40°C to 125°C; unless otherwise noted.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Over Current Protection (OCP) Sensing Section						
Over Current Protection (OCP) threshold percentage of maximum current	PD request for constant voltage mode with VBUS at 5.2 V and 3 A maximum current	$I_{OCP-PER}$	109	120	124	%
OCP debounce time	Constant current exceeding $I_{OCP-PER}$	$t_{OCP-DEB}$	50	60	70	ms
Current threshold on sensing resistor for enabling discharge on DISC pin during a voltage transition	VBUS is decreasing	$I_{CS-DSCG}$		430		mA
Debounce time for enabling discharge on DISC pin during a voltage transition	VBUS is decreasing	$t_{CS-DSCG}$		0.6	1.0	ms
Constant Voltage Sensing Section						
VFB Reference Voltage at 3.3 V	VBUS = 3.3 V, current sense resistor voltage, Vcs = 0 V	$V_{CVR-3.3V}$	0.32	0.33	0.34	V
VFB Reference Voltage at 5.2 V nominal output voltage	VBUS = 5.2 V, current sense resistor voltage, Vcs = 0 V	V_{CVR-5V}	0.504	0.520	0.536	V
VFB Reference Voltage at 9 V nominal output voltage	VBUS = 9 V, current sense resistor voltage, Vcs = 0 V	V_{CVR-9V}	0.873	0.900	0.927	V
VFB Reference Voltage at 15 V nominal output voltage	VBUS = 15 V, current sense resistor voltage, Vcs = 0 V	$V_{CVR-15V}$	1.455	1.500	1.545	V
VFB Reference Voltage at 20 V nominal output voltage	VBUS = 20 V, current sense resistor voltage, Vcs = 0 V	$V_{CVR-20V}$	1.940	2.000	2.060	V
Feedback Section						
CATH(FB) pin sink/source current (Note 5)	CATH(FB) as a sink (Note 6)	$I_{CATH-SNK}$	2			mA
CATH(FB) pin sink/source current (Note 5)	CATH(FB) as a source (Note 6)	I_{FB-SRC}			−2	mA
Discharge Section						
VBUS to GND Leakage Resistance	DC_EN = 0 V, VBUS not sourced	$R_{DISC-VBUS}$	72.4	155		kΩ
VBUS Pin Sink Current	VBUS = 20 V and being discharged	$I_{DISC-SNK}$	250			mA
Discharge Time	During VBUS voltage transition of voltage step ≤ 0.5 V, final V_{VBUS} > 13 V	$t_{DISC-11}$	5.5	7	8.5	ms
Discharge Time	During VBUS voltage transition of voltage step ≤ 0.5 V, final V_{VBUS} < 13 V	$t_{DISC-10}$	51	55	60	ms
Discharge Time	During VBUS voltage transition of voltage step > 0.5 V, final V_{VBUS} > 13 V					

APPLICATIONS INFORMATION

FUSB3317 has the entire Power Delivery (PD) communication stack within hardware including the

Figure 8. Voltage and Current Sensing Circuits

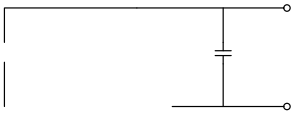


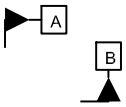
Figure 9. Protection Block Diagram

PDIV0, PDIV1

These pins are prepared in addition to the fuse bits to provide a

REFERENCES AND DEFINITIONS

QFNW20 4x4, 0.5P



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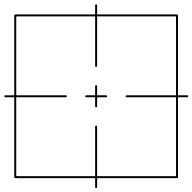
TOP VIEW



GENERIC
MARKING DIAGRAM*