USB Type-C Port Controller with USB-PD

FUSB308B

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BLOCK DIAGRAM

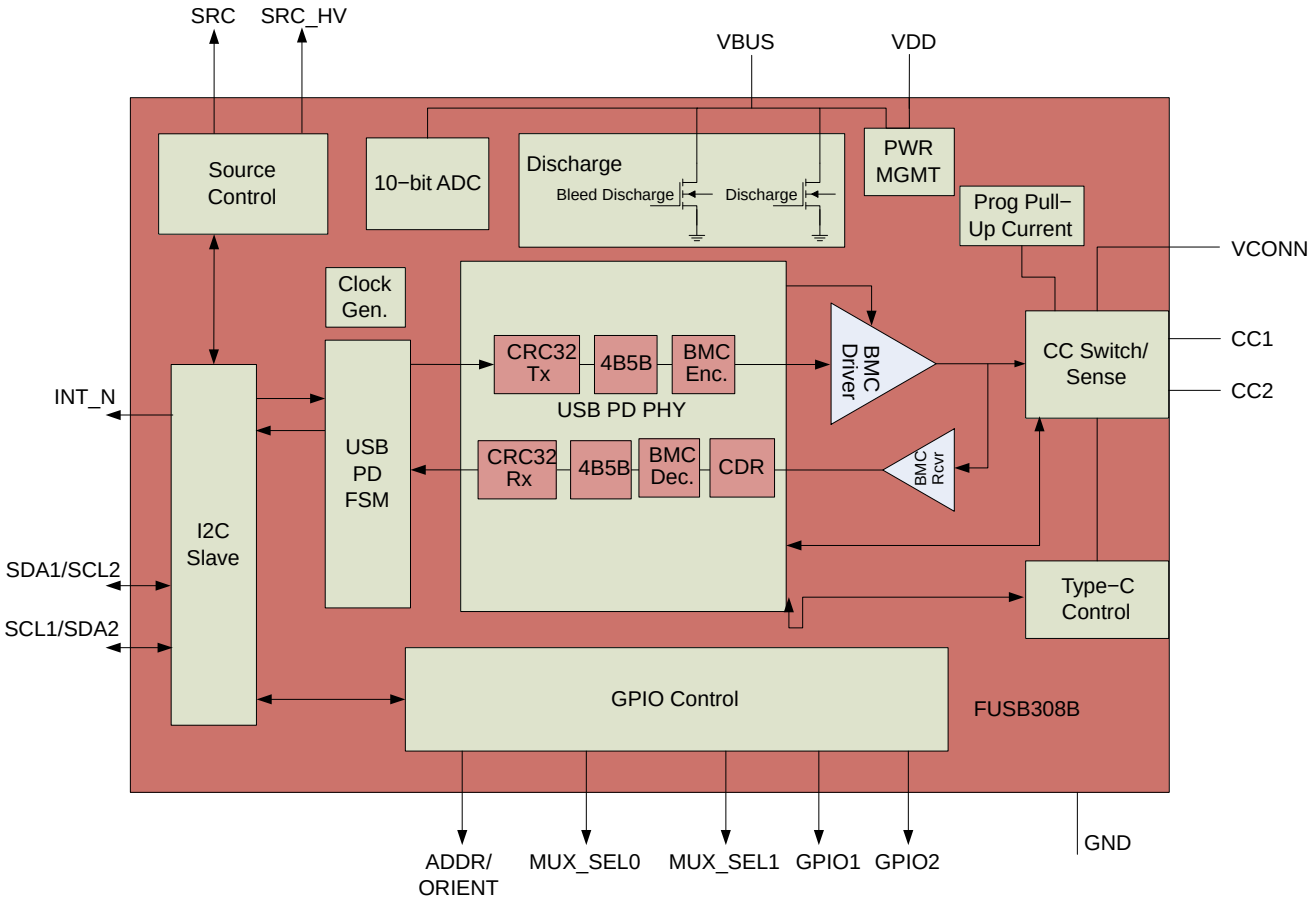

Figure 2. FUSB308B Block Diagram

PIN CONFIGURATIONS

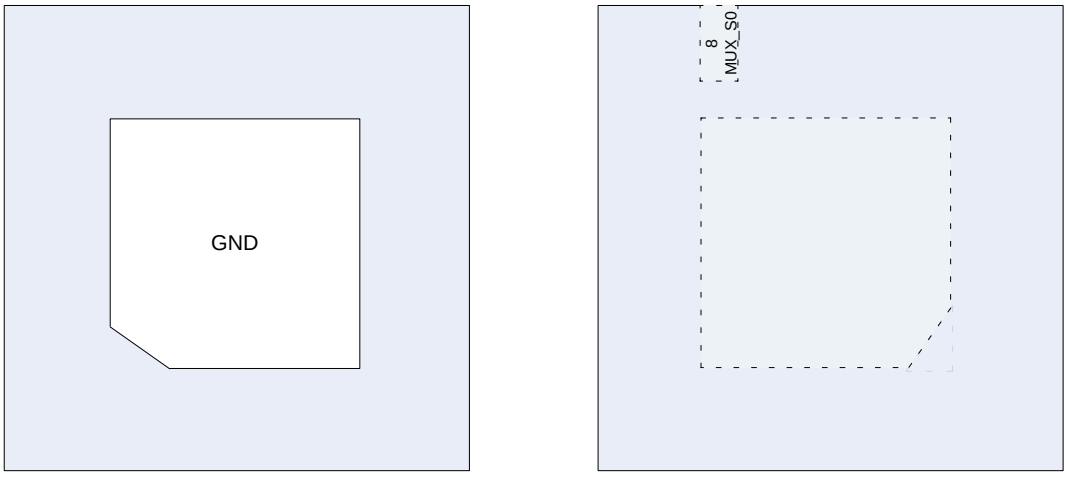

Figure 3. Pin Assignment QFN (FUSB308B)

PIN DESCRIPTIONS

Table 2. PIN DESCRIPTION

Name	Type	Description
USB TYPE−C CONNECTOR INTERFACE		
CC1	I/O	Type−C connector Configuration Channel (CC) pins. Initially used to determine when an attach has occurred and what the orientation of the insertion is. Functionality after attach depends on mode of operation detected. Operating as a host: − Sets the allowable charging current for VBUS to be sensed by the attached device − Used to communicate with devices using USB BMC Power Delivery − Used to detect when a detach has occurred Operating as a device: − Indicates what the allowable sink current is from the attached host − Used to communicate with devices using USB BMC Power Delivery
CC2	I/O	
GND	Ground	Ground
VBUS	Power	VBUS supply pin for attach and detach detection when operating as an upstream facing port (Device)
POWER INTERFACE		
VDD	Power	Input supply voltage
GPIO2	3−State CMOS I/O	General Purpose I/O
VCONN	Power Switch	Regulated input to be switched to correct CC pin as VCONN to power USB3.1 fully featured cables, powered accessories or dongles bridging Type C to other video or audio connectors
SIGNAL INTERFACE		
SCL1/SDA2 (Note 1)	Open−Drain I/O	I^2C serial clock/data signal to be connected to the I^2C master
SDA1/SCL2 (Note 1)	Open−Drain I/O	I^2C serial clock/data signal to be connected to the I^2C master
INT_N	Open−Drain Output	Active LOW open drain interrupt output used to prompt the processor to read the I^2C register bits
ORIENT/I2C_ ADDR (Note 1)	3−State CMOS Output	Selects I^2C Address on Power up and then becomes a General Purpose CMOS Output
MUX_SEL0	3−State CMOS Output	MUX Selection Output 0
MUX_SEL1	3−State CMOS I/O	MUX Selection Output 1
GPIO1	[redacted]	

I²C IDLE MODE

Entering I²C Idle Mode

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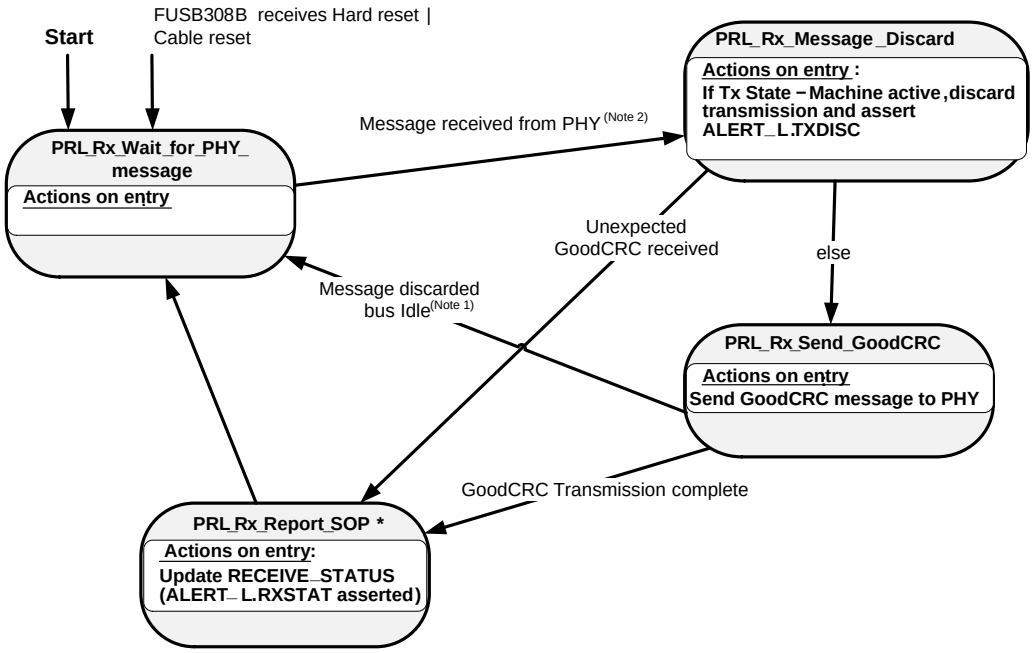

2. This indication is sent by the PHY when a message has been discarded due to CC being busy, and after CC becomes idle again (see USB PD Spec).
3. Messages do not include Hard Reset or Cable Reset signals or expected GoodCRC messages (GoodCRC messages are only expected after the FUSB308B PHY has received the tx message and the FUSB308B Tx state−machine is in the PRL_Tx_Wait_for_PHY_response state).

Figure 6. Receive State Machine

TRANSMIT STATE MACHINE

HARD RESET/ CABLE RESET STATE MACHINE

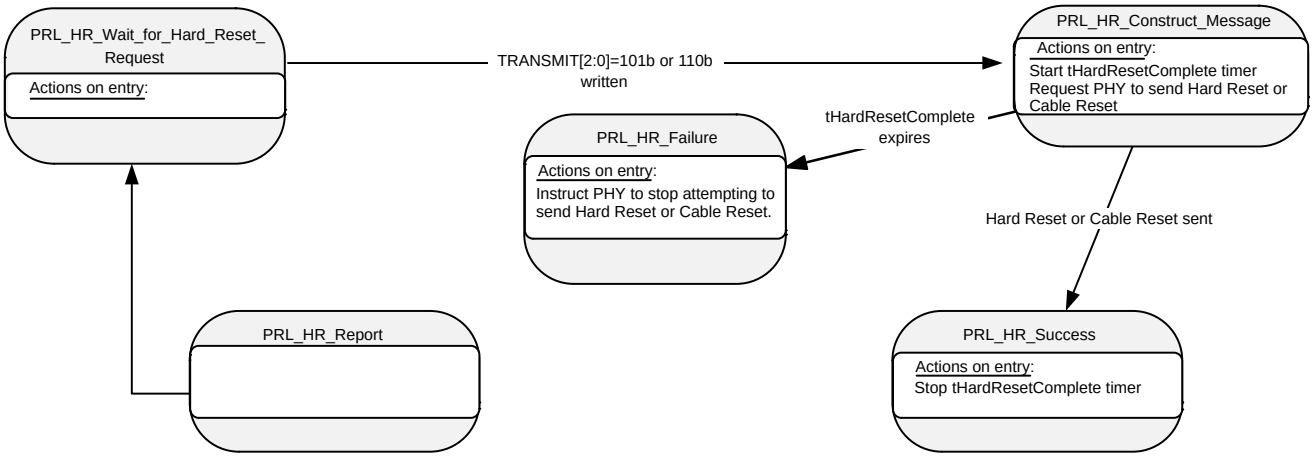

Figure 8. Hard Reset and Cable Reset State Machine

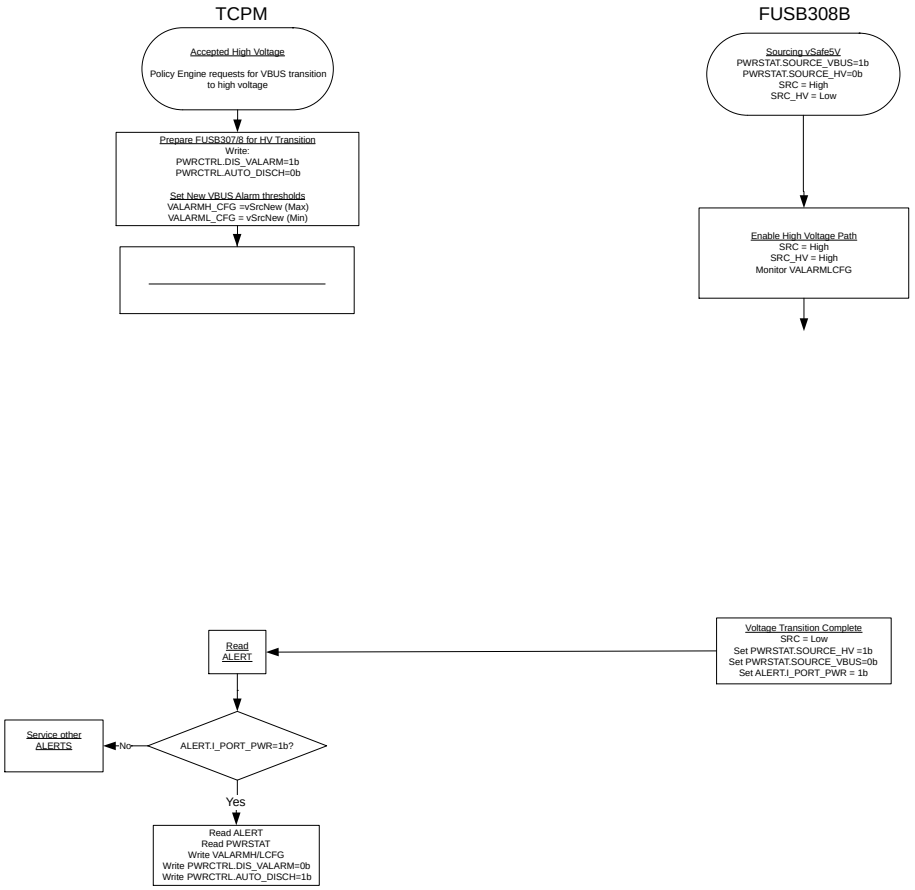

Figure 10. Transition to High Voltage Sourcing using SRC_HV Controlled Path (FUSB308B)

Figure 11. Transition to vSafe5V from SRC_HV Controlled Path (FUSB308B)

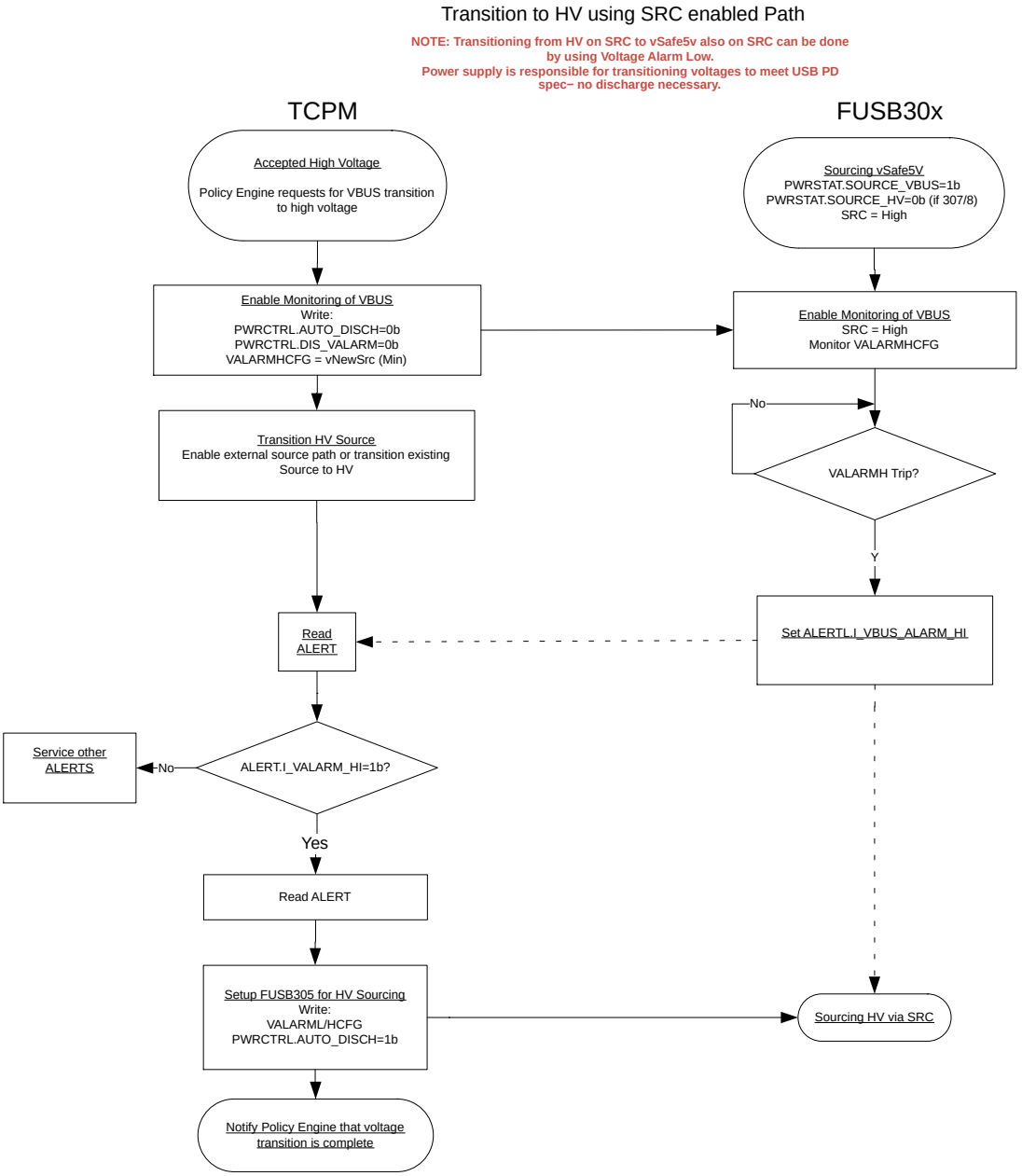

Figure 12. Transition to High Voltage using SRC Controlled Path VBUS

VBUS MONITORING AND MEASUREMENT

DISCHARGE DURING A CONNECTION

– R_{FULL_DISCH}.

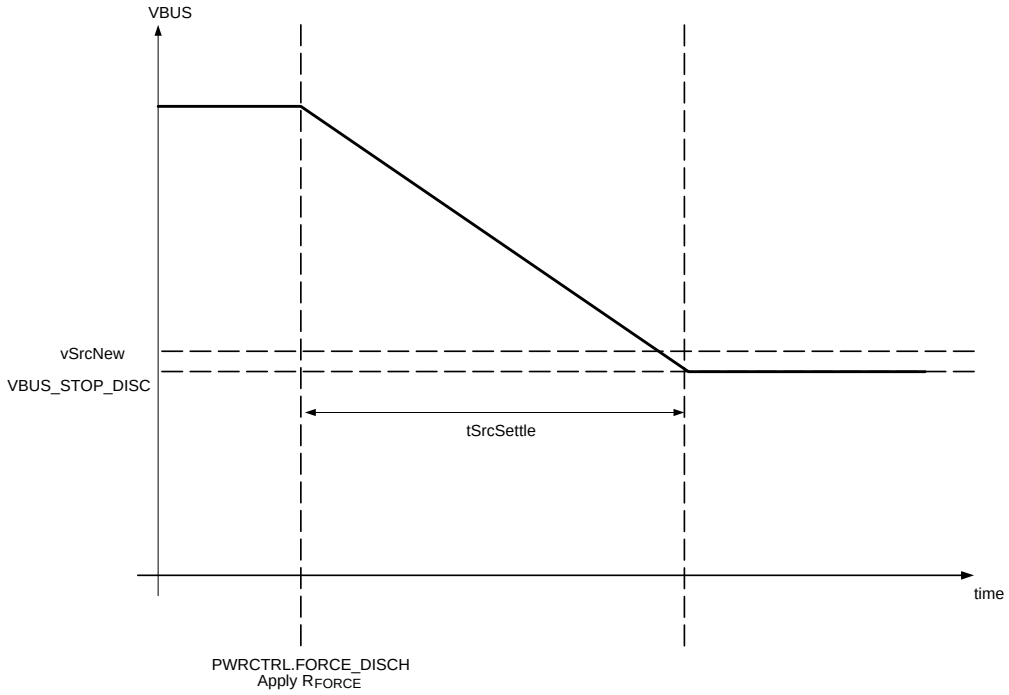

Figure 14. Source Discharge During a Connection

WATCHDOG TIMER

DC AND TRANSIENT CHARACTERISTICS

CURRENT CONSUMPTION

Symbol	Parameter	T_A = −40 to +85°C T_A = −40 to +105°C (Note 15) T_J = −40 to +125°C			Unit
		Min	Typ	Max	
$I_{DISABLE}$	Disable Current (ROLECTRL = 0x0F)			10	μA
	Unattached DRP or Source		7	20	μA
	Attached as Source (No PD)		12	22	μA

BASEBAND PD

Symbol	Parameter	T_A = −40 to +85°C T_A = −40 to +105°C (Note 15) T_J = −40 to +125°C			Unit
		Min	Typ	Max	
UI	Unit Interval	3.03	3.33	3.70	μs

TRANSMITTER

zDriver	TX output impedance at 750 kHz with an external 220 pF or equivalent load	33		75	Ω
tEndDriveBMC	Time to cease driving the line after the end of the last bit of the Frame			2	UI
tHoldLowBMC	Time to cease driving the line after the final high−to−low transition	1			μs

VBUS MEASUREMENT CHARACTERISTICS (continued)

Symbol	Parameter	T_A = −40 to +85°C T_A = −40 to +105°C (Note 15) T_J = −40 to +125°C			Unit
		Min	Typ	Max	
vSafe0Vthr	Safe Operating Voltage at “Zero Volts” Threshold			0.8	V
vSafe0Vhys	vSafe0V Hysteresis		40		mV
vALARMLSB	LSB of VBUS thresholds for VBUS_SNK_DISCL VBUS_STOP_DISCL VALARMHCFGL VALARMLCFGL		50		mV
pALARM	Accuracy of VBUS thresholds for VBUS_SNK_DISCL VBUS_STOP_DISCL VALARMHCFGL VALARMLCFGL			±5	%

SOURCE AND SINK CONTROL SPECIFICATIONS

Symbol	Parameter		T_A = −40 to +85°C, T_A = −40 to +105°C (Note 15), T_J = −40 to +125°C			
			Min	Typ	Max	Unit
R_{BLEED}	Equivalent Resistance for bleed discharging VBUS	VBUS = 4.0 V to 21.5 V	4		7	kΩ
vSrcSlewNeg	Maximum slew rate allowed when discharging VBUS	VBUS = 4.0 V to 21.5 V			30	mV/μs
tSafe0V	Time to reach vSafe0V max				650	ms
tSafe5V	Time to reach vSafe5V max				275	ms

OVER-TEMPERATURE SPECIFICATIONS

Symbol	Parameter	Min	Typ	Max	Unit
T_{SHUT}	Temp. for VCONN Switch Turn Off		145		°C
T_{HYS}	Temp. Hysteresis for VCONN Switch Turn On		10		°C

WATCHDOG TIMER SPECIFICATIONS

Symbol	Parameter	Min	Typ	Max	Unit

IO SPECIFICATIONS (continued)

Symbol	Parameter	V_{DD} (V)	Conditions	T_A = −40 to +85°C T_A = −40 to +105°C (Note 15) T_J= −40 to +125°C Min	Typ	Max	Unit
SRC, SNK AND SRC_HV							
V_{OH}	High−Level Output Voltage	3.0 to 5.5	I_{OH} = −2 mA	$0.7V_{DD}$			V
I^2C INTERFACE PINS – STANDARD, FAST OR FAST MODE PLUS SPEED MODE SDA, SCL) (Note 13)							
V_{DDEXT}	External power supply to which SDA and SCL are pulled up			1.8		3.6	V
V_{ILI2C}	Low−Level Input Voltage	3.0 to 5.5				0.4	V
V_{IHI2C}	High−Level Input Voltage	3.0 to 5.5		1.2			V
V_{HYS}	Hysteresis of Schmitt Trigger Inputs	3.0 to 5.5		0.2			V
I_{i2C}	Input Current of SDA and SCL Pins,	3.0 to 5.5	Input Voltage 0.26 V to 2 V	−			

Table 4. REGISTER DEFINITIONS

Address	R[illegible]	[illegible]Type	[illegible]Rst Val	[illegible]Bit7	[illegible]Bit6	[illegible]Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00h	VENDIDL	R	79h	Vendor ID Low							
01h	VENDIDH	R	07h	Vendor ID High							
02h	PRODIDL	R	34h								

Table 4. REGISTER DEFINITIONS (continued)

Address	Register Name	Type	Rst Val	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
1Bh	FAULTCTRL	R/W	00h	Reserved			Reserved	DISCH_TIMER_DIS	Reserved	Reserved	VCONN_OCP_DIS
1Ch	PWRCTRL	R/W	60h	Reserved	VBUS_MON	DIS_VALRM	AUTO_DISCH	EN_BLEED_DISCH	FORCE_DISCH	VCONN_PWR	EN_VCONN
1Dh	CCSTAT	R	00h/20h	Reserved		LOOK4CON	CON_RES	CC2_STAT		CC1_STAT	
1Eh	PWRSTAT	R	08h	DEBUG_ACC	TCPC_INIT	SOURCE_HV	SOURCE_VBUS	VBUS_VAL_EN	VBUS_VAL	VCONN_VAL	SNKVBUS
1Fh	FAULTSTAT	R	80h	ALL_REGS_RESET	Reserved	AUTO_DISCH_FAIL	FORCE_DISCH_FAIL	Reserved	Reserved	VCONN_OCP	I2C_ERR
20h..22h	Reserved	R	00h	Reserved							
23h	COMMAND	R	00h	Command							
24h	DEVCAP1L	R	DDh	ROLES_SUPPORT			ROLES_SUPPORT	SWITCH_VCONN	SNK_VBUS	SRC_HV	SRC_VBUS
25h	DEVCAP1H	R	1Eh	Reserved			BLEED_DIS	FORCE_DIS	VBUS_MEAS_ALRM	RP_SUPPORT	
26h	DEVCAP2L	R	D7h	SNK_DISC_DETECT	STOP_DISCH	VBUS_ALRM_LSB		VCONN_POWER_CAP			VCONN_FAULT_CAP
27h	DEVCAP2H	R	01h	Reserved							Watchdog Timer
28h	STD_IN_CAP	R	00h	Reserved							
29h	STD_OUT_CAP	R	41h	Reserved	DEBUG_ACC	Reserved			MUX_CTRL	Reserved	ORIENT
2Ah..2Dh	Reserved	R	00h	Reserved							
2Eh	MSGHEADR	R/W	02h	Reserved			Cable Plug	Data Role	USB PD Rev		PWR Role
2Fh	RXDETECT	R/W	00h	Reserved	EN_CABLE_RST	EN_HRD_RST	EN_SOP2_DBG	EN_SOP1_DBG	EN_SOP2	EN_SOP1	EN_SOP
30h	RXBYTECNT	R	00h	Received Byte Count							
31h	RXSTAT	R	00h	Reserved					Received SOP* Message		
32h	RXHEADL	R	00h	Received Header Low							
33h	RXHEADH	R	00h	Received Header High							
34h..4Fh	RXDATA	R	00h	Received Data Payload							
50h	TRANSMIT	R/W	00h	Reserved		Retry Counter		Reserved	Transmit SOP* Message		

Table 4. REGISTER DEFINITIONS (continued)

Address	Register Name	Type	Rst Val	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
51h	TXBYTECNT	R/W	00h	Transmit Byte Count							
52h	TXHEADL	R/W	00h	Transmit Header Low							
53h	TXHEADH	R/W	00h	Transmit Header High							
54h..6F	TXDATA	R/W	00h	Transmit Payload							
70h	VBUS_VOLTAGE_L	R	00h	VBUS Measurement Output							
71h	VBUS_VOLTAGE_H	R	00h								
72h	VBUS_SNK_DISCL	R/W	A0h	VBUS SINK Disconnected Threshold (See Register Description Table)							
73h	VBUS_SNK_DISCH	R/W	1Ch								
74h											

Table 5. VENDIDL
Address: 00h
Reset Value: 0x79
Type: Read

Bit #	Name	R/W/C	Size (Bits)	Vendor ID Low Description
7:0	VENDIDL	R	8	ON Semiconductor Vendor ID Low: **79h**

Table 6. VENDIDH
Address: 01h
Reset Value: 0x07
Type: Read

Bit #	Name	R/W/C	Size (Bits)	Vendor ID High Description
7:0	VENDIDH	R	8	ON Semiconductor Vendor ID High: 07h

Table 7. PRODIDL
Address: 02h
Reset Value: See Below
Type: Read

Bit #	Name	R/W/C	Size (Bits)	Product ID Low Description
7:0	PRODIDL	R	8	Product ID Low, **FUSB308B: 34h**

Table 8. PRODIDH
Address: 03h
Reset Value: 0x01h
Type: Read

Bit #	Name	R/W/C	Size (Bits)	Product ID High Description
7:0	PRODIDH	R	8	Product ID High, **All: 1h**

Table 9. DEVIDL
Address: 04h
Reset Value: 0x02h
Type: Read

Bit #	Name	R/W/C	Size (Bits)	Device ID Low (Version) Description
7:0	REVIDL	R	8	Revision ID Low: **01h** **A_[Revision ID]: 0x01 (e.g. A_revA**) B_[Revision ID]: 0x02 **(e.g. B_revA)** C_[Revision ID]: 0x03 **(e.g. C_revA)** etc

Table 10. DEVIDH
Address: 05h
Reset Value: 0x02h
Type: Read

Bit #	Name	R/W/C	Size (Bits)	Device ID High (Revision) Description
7:0	DEVIDH	R	8	Revision ID High: **00h**" **[Version ID]_revA: 0x00 (e.g. A_revA)** [Version ID]_revB: 0x01 **(e.g. A_revB)** [Version ID]_revC: 0x02 **(e.g. A_revC)** etc

Table 11. TYPECREVL
Address: 06h
Reset Value: 0x12h
Type: Read

Bit #	Name	R/W/C	Size (Bits)	Type−C Revision Low Description
7:0	TYPECREVL	R	8	Type−C Revision High: **12h**

Table 12. TYPECREVH
Address: 07h
Reset Value: 0x00h
Type: Read

Bit #	Name	R/W/C	Size (Bits)	Type−C Revision High Description
7:0	TYPECREVH	R	8	Type−C Revision High: **00h**

Table 13. USBPDVER
Address: 08h
Reset Value: 0x12h
Type: Read

Bit #	Name	R/W/C	Size (Bits)	USB−PD Version Description
7:0	USBPDVER	R	8	USB−PD Version: **12h**

Table 14. USBPDREV
Address: 09h
Reset Value: 0x20h
Type: Read

Bit #	Name	R/W/C	Size (Bits)	USB−PD Revision Description
7:0	USBPDREV	R	8	USB−PD Revision: **20h**

Table 15. PDIFREVL
Address: 0Ah
Reset Value: 0x12h
Type: Read

Bit #

Table 17. ALERTL
Address: 10h
Reset Value: 0x00
Type: Read, Write 1 to Clear

Bit #	Name	R/W/C	Size (Bits)	ALERT1 Description

Table 18. ALERTH

Address: 11h

Reset Value: 0x00

Type: Read, Write 1 to Clear

Bit #	Name	R/W/C	Size (Bits)	ALERT2 Description
7	I_VS_ALERT	RWC	1	Vendor Defined Alert 0b: Cleeared 1b: A Vendor Defined Alert occurred. Please read ALERT_VD register
6:4	Reserved	R	3	**Reserved: 000b**
3	I_VBUS_SNK_DISC	RWC	1	VBUS Sink Disconnect Detected **0b: Cleared** 1b: A VBUS Sink Disconnect Threshold crossing from High to Low has been detected
2	I_RX_FULL	RWC	1	Rx Buffer Overflow **0b: Internal RX Buffer is functioning properly** 1b: Internal RX Buffer has overflowed Note: This interrupt indicates overflow of the internal buffer, not the RXDATA space. To clear overflow condition, write to ALERTL.I_RX-STAT Writing a 1 to this register acknowledges the overflow. The actual overflow is cleared by writing to ALERTL. I_RXSTAT
1	I_FAULT (Note 17)	R/WC	1	Fault Alarm **0b: Cleared** 1b: A Fault alarm has occurred. Read FAULTSTAT register
0	I_VBUS_ALRM_LO	R/WC	1	Voltage Alarm Lo **0b: Cleared** 1b: A low−voltage alarm has occurred

17. ALERTH.I_FAULT is asserted if the bit−

Table 20. ALERTMSKH

Address: 13h

Reset Value: 0xFF (Resets on POR, SW_RST and Hard Reset)

Type: Read/Write

Bit #	Name	R/W/C	Size (Bits)	Alert Mask 2 Description
7	M_VD_ALERT	RW	1	0b: Interrupt masked, **1b: Interrupt unmasked**
6:4	Reserved	R	3	**Reserved: 000b**
3	M_VBUS_SNK_DISC	RW	1	0b: Interrupt masked, **1b: Interrupt unmasked**
2	M_RX_FULL	RW	1	0b: Interrupt masked, **1b: Interrupt unmasked**
1	M_FAULT	RW	1	0b: Interrupt masked, **1b: Interrupt unmasked**
0	M_VBUS_ALRM_LO	RW	1	0b: Interrupt masked, **1b: Interrupt unmasked**

Table 22. FAULTSTATMSK

Address: 15h
Reset Value: 0x33 (Resets on POR, SW_RST and Hard Reset)
Type: Read/Write

Bit #	Name	R/W/C	Size (Bits)	Fault Status Mask Description
7	M_ALL_REGS_RESET	RW	1	All Registers Reset to Default 0b: Interrupt masked **1b: Interrupt unmasked**
6	Reserved	R	1	**Reserved: 0b**
5	M_AUTO_DISCH_FAIL	RW	1	Auto Discharge Fail Interrupt Mask 0b: Interrupt masked **1b: Interrupt unmasked**
4	M_FORCE_DISCH_FAIL	RW	1	Force Discharge Fail Interrupt Mask 0b: Interrupt Masked **1b: Interrupt Unmasked**
3	Reserved	R	1	**Reserved: 0b**
2	Reserved	R	1	**Reserved: 0b**
1	M_VCONN_OCP	RW	1	VCONN OCP Interrupt Mask 0b: Interrupt Masked **1b: Interrupt Unmasked**
0	M_I2C_ERROR	RW	1	I2C Interface Error Interrupt Mask 0b: Interrupt Masked **1b: Interrupt Unmasked**

Table 23. STD_OUT_CFG

Address: 18h
Reset Value: 0x40
Type: Read/Write

Bit #	Name	R/W/C	Size (Bits)	Standard Outputs Configuration
7	TRI_STATE	R/W	1	**0b: Standard Output Control** 1b: Force all outputs to tri−state
6	Reserved	R/W	1	**Reserved: 0b**
5	Reserved	R	1	**Reserved: 0b**
4	Reserved	R	1	**Reserved: 0b**
3:2	MUX_CTRL	R/W	2	Controls MUX_S0 and MUX_S1 Outputs. **00b: MUX_S0 = 0, MUX_S1 = 0. No connection.** 01b: MUX_S0 = 1, MUX_S1 = 0. *USB3.1 Connected* 10b: MUX_S0 = 0, MUX_S1 = 1. *DP Alternate Mode – 4 lanes* 11b: MUX_S0 = 1, MUX_S1 = 1. USB3.*1 + Display Port Lanes 0 & 1*
1	Reserved	R	1	**Reserved: 0b**
0	ORIENT	R/W	1	Controls ORIENT Output **0b: Normal (CC1 = A5, CC2 = B5, TX1 = A2/A3, RX1 = B10/B11)** 1b: Flipped (CC2 = A5, CC1 = B5, TX1 = B2/B3, RX1 = A10/A11)

Table 24. TCPC_CTRL

Address: 19h

Reset Value: 0x00 (POR, and SW_RST)

Type: Read/Write

Bit #	Name	R/W/C	Size (Bits)	TCPC Control Register
7:4	Reserved	R		
5	EN_WATCHDOG	R/W	1	**0b: Watchdog Monitoring isTRL**

Table 26. FAULTCTRL
Address: 1Bh
Reset Value: 0x00
Type: Read/Write

Bit #	Name	R/W/C	Size (Bits)	Fault Control Description
7:4	Reserved	R	4	**Reserved: 0000b**
3	DISCH_TIMER_DIS	R/W	1	Auto and Force VBUS Discharge Timer Enable **0b: VBUS Discharge timer is enabled** 1b: VBUS Discharge timer is disabled
2	Reserved	R	1	**Reserved: 0b**
1	Reserved	R	1	**Reserved: 0b**
0	VCONN_OCP_DIS	R/W	1	VCONN OCP Enable **0b: VCONN OCP Enabled** 1b: VCONN OCP Disabled

Table 27. PWRCTRL
Address: 1Ch
Reset Value: 0x60
Type: Read/Write

Bit #	Name	R/W/C	Size (Bits)	Power Control Description
7	Reserved	R	1	**Reserved: 0b**
6	DIS_VBUS_MON (Note 23)	R/W	1	Controls **VBUS_VOLTAGE_L** Monitoring. 0b: VBUS Voltage Monitoring is enabled **1b: VBUS Voltage Monitoring is disabled**
5	DIS_VALARM	R/W	1	Disables **VALARMHCFGL** and **VALARMLCFGL** 0b: Voltage Alarm reporting is enabled **1b:Voltage Alarm reporting is disabled**
4	AUTO_DISCH (Notes 24, 26)	R/W	1	Auto Discharge on Disconnect 0b: Turn Off Automatically Discharge VBUS based on VBUS Voltage **1b: Turn On Automatically Discharge VBUS based on VBUS Voltage**
3	EN_BLEED_DISCH (Note 28)	R/W	1	Enable Bleed Discharge **0b: Disable bleed discharge of VBUS** 1b: Enable bleed discharge of VBUS
2	FORCE_DISCH (Note 25, 27)	R/W	1	Force Discharge **0b: Disable forced discharge of VBUS** 1b: Enable forced discharge of VBUS
1	VCONN_PWR	R/W	1	VCONN Power Supported **Writing this bit has no function. Please use VCONN_OCP to set OCP values**
0	EN_VCONN	R/W	1	Enable VCONN 0b: Disable VCONN Source (default) 1b: Enable VCONN Source to CC

23. If VBUS_MON is disabled, VBUS_VOLTAGE_L and VBUS_VOLTAGE_H reports all zeroes.

Table 28. CCSTAT
Address: 1Dh
Reset Value: 0x00
Type: Read

Bit #	Name

Table 29. PWRSTAT

Address: 1Eh

Reset Value: 08h

Type: Read

Bit #	Name	R/W/C	Size (Bits)

Table 30. FAULTSTAT (continued)
Address: 1Fh
Reset Value: 0x80
Type: Read/Write 1 to Clear

Bit #	Name	R/W/C	Size (Bits)	Fault Status Interrupt Description (Note 32)
4	FORCE_DISCH_FAIL	R/WC	1	

Table 31. COMMAND (continued)
Address: 23h

Table 32. DEVCAP1L (continued)
Address: 24h
Reset Value: FUSB308B: DBh
Type: Read

Bit #	Name	R/W/C	Size (Bits)	Device Capabilities 1 L Description
3	SWITCH_VCONN	R	1	Supply VCONN: 0b: Not capable of switching VCONN **1b: Capable of switching VCONN** Support for PWRSTAT.VCONN_VAL and PWRCTRL.EN_VCONN implemented
2	SNK_VBUS	R	1	Sink VBUS: 0b: Not Capable of controlling the sink path to the system load 1b: Capable of controlling the sink path to the system load Support for PWRSTAT.SNKVBUS and COMMAND.SinkVbus implemented
1	SRC_HV	R	1	Source Higher than vSafe5V on VBUS 0b: Not capable of controlling High Voltage Path on VBUS 1b: capable of controlling High Voltage Path on VBUS Support for PWRSTAT.SOURCE_HV and COMMAND.SourceVbusHighVoltage implemented
0	SRC_VBUS	R	1	Source vSafe5V on VBUS 0b: Not of controlling the source path to VBUS **1b: Capable of controlling the source path to VBUS** Support for PWRSTAT.SOURCE_VBUS, COMMAND.SourceVbusDefaultVoltage, COMMAND.DisableSourceVbus, COMMAND.EnableVbusDetect, and COMMAND.DisableVbusDetect implemented

Table 33. DEVCAP1H
Address: 25h
Reset Value: 0x1E
Type: Read

Bit #	Name	R/W/C	Size (Bits)	Device Capabilities 1 H Description
7:5	Reserved	R	3	**Reserved : 000b**
4	BLEED_DIS	R	1	0b: No Bleed Discharge **1b: Bleed Discharge implement** Support for PWRCTRL.EN_BLEED_DISCH implemented.
3	FORCE_DIS	R	1	0b: No Force Discharge **1b: Force Discharge implement** Support for PWRCTRL.FORCE_DISCH, FAULTSTAT.FORCE_DISCH_FAIL, and VBUS_STOP_DISCL implemented
2	VBUS_MEAS_ALRM	R	1	**0b: No VBUS voltage measurement or VBUS Alarms** **1b: VBUS voltage measurement and VBUS Alarms** Support for VBUS_VOLTAGE_L, VALARMHCFGL and VALARMLCFGL implemented
1:0	RP_SUPPORT	R	2	Source Power Supported: 00b: Rp default only 01b: Rp 1.5 A and default **10b: Rp 3.0A, 1.5 A and default** 11b: Reserved

Table 34. DEVCAP2L

Address: 26h
Reset Value: 0xD7
Type: Read

Bit #	Name	R/W/C	Size (Bits)	Device Capabilities 2 L Description
7	SNK_DISC_DETECT	R	1	0b: **VBUS_SNK_DISCL not implemented** **1b: VBUS_SNK_DISCL implemented**
6	STOP_DSICH	R	1	0b: **VBUS_STOP_DISCL** not implemented **1b: VBUS_STOP_DISCL implemented**
5:4	VBUS_ALRM_LSB	R	2	VBUS Voltage Alarm LSB Support **01b: Voltage Alarm Supports 50 mV LSB** Bit 0 of VALARMHCFGL and VALARMLCFGL are ignored
3:1	VCONN_POWER_CAP	R	3	VCONN Power Supported 000b: 1.0 W 001b: 1.5 W 010b: 2.0 W **011b: 3 W (at VCONN = 5.5 V)** 100b: 4 W 101b: W Reset Value:80xD7

Table 37. MSGHEADR

Address: 2Eh
Reset Value: FUSB308B: 0x0B
Type: Read/Write

Bit #	Name	R/W/C	Size (Bits)	Message Header Info Description
7:5	Reserved	R	3	Reserved: 000b
4	CBL_PLUG	R/W	1	Cable Plug **0b: Message originated from Source, Sink, or DRP** 1b: Message originated from a Cable Plug
3	DATA_ROLE	R/W	1	Data Role **0b: SINK** 1b: SOURCE
2:1	USBPD_REV	R/W	2	USB−PD Specification Revision 00b: Revision 1.0 **01b: Revision 2.0** 10b – 11b: Reserved
0	POWER_ROLE	R/W	1	Power Role **0b: Sink** 1b: Source

Table 38. RXDETECT

RXDETECT enables the types of messages and/or signaling to be detected. SOP* enabling also turns on auto−GoodCRC response. This register is reset when: A Hard Reset is received or sent; after the GoodCRC transmission due to RxOneMore; on a disconnect detection; SW_RST or POR.

Address: 2Fh
Reset Value: 0x00
Type: Read/Write

Bit #	Name	R/W/C	Size (Bits)	Receive Detect Description (Note 34)
7	Reserved	R	1	**Reserved: 0b**
6	EN_CABLE_RST	R	1	**0b: Do not detect Cable Reset signaling**
5	EN_HRD_RST	R/W	1	**0b: Do not detect Hard Reset signaling (default)** 1b: Detect Hard Reset signaling
4	EN_SOP2_DBG	R/W	1	**0b: Do not detect SOP_DBG” message (default)** 1b: Detect SOP_DBG” message
3	EN_SOP1_DBG	R/W	1	**0b: Do not detect SOP_DBG’ message (default)** 1b: Detect SOP_DBG’ message
2	EN_SOP2	R/W	1	**0b: Do not detect SOP” message (default)** 1b: Detect SOP” message
1	EN_SOP1	R/W	1	**0b: Do not detect SOP’ message (default)** 1b: Detect SOP’ message
0	EN_SOP	R/W	1	**0b: Do not detect SOP message (default)** 1b: Detect SOP message

34. Writing all 0s to this register disables PD.

Table 39. RXBYTECNT

Address: 30h
Reset Value: 0x00
Type: Read

Bit #	Name	R/W/C	Size (Bits)	Received Byte Count Description
7:0	RXBYTECNT	R	8	**Number of Bytes Received. This is the number of bytes in RX-DATA plus 3 (RXSTAT and RXHEADL, H)**

Table 44. TRANSMIT (continued)
Writing this register will start a PD transmission. If Cable Reset, Hard Reset or BIST Carrier Mode 2 is written, RETRY_CNT is ignored and signaling is not retried.
Address: 50h
Reset Value: 0x00
Type: Read/Write

Bit #	Name	R/W/C	Size (Bits)	Transmit Description
3	Reserved	R	1	Reserved: 0b
2:0	TXSOP	R/W	3	**Transmit SOP Message** **000b: Transmit SOP** 001b: Transmit SOP' 010b: Transmit SOP'' 011b: Transmit SOP_DBG' 100b: Transmit SOP_DBG'' 101b: Transmit Hard Reset 110b: Transmit Cable Reset 111b: Transmit BIST Carrier Mode 2 (Enabled for *tBISTContMode*)

Table 45. TXBYTECNT
Address: 51h
Reset Value: 0x00
Type: Read/Write

Bit #	Name	R/W/C	Size (Bits)	Transmit Byte Count Description
7:0	TXBYTECNT	R/W	8	**Number of bytes to be transmitted**

Table 46. TXHEADL
Address: 52h
Reset Value: 0x00
Type: Read/Write

Bit #	Name	R/W/C	Size (Bits)	Transmit Header Low Description
7:0	TXHEADL	R/W	8	**Transmit Header Low**

Table 47. TXHEADH
Address: 53h
Reset Value: 0x00
Type: Read/Write

Bit #

Table 49. VBUS_VOLTAGE_L
Address: 70h
Reset Value: 0x00
Type: Read

Bit #	Name	R/W/C	Size (Bits)	VBUS Voltage Low Description
Byte 27:0	TX_Data27..0	RW	8	**TX Payload**

Table 50. VBUS_VOLTAGE_H
Address: 71h
Reset Value: 0x00
Type: Read

Bit #	Name	R/W/C	Size (Bits)	VBUS Voltage High Description (Note 35)
7:4	Reserved	R	4	**Reserved: 0000b**
3:2	VBUS_SCALE	R	2	**00b: VBUS Measurement not scaled** 01b: VBUS Measurement divided by 2 10b: VBUS Measurement divided by 4 11b: Reserved
1	VBUS_V_BIT9	R	1	Bit 9 of VBUS Measurement
0	VBUS_V_BIT8	R	1	Bit 8 of VBUS Measurement

35. VBUS_V_BIT[9:0] is the measured VBUS voltage divided by VBUS_SCALE factor.

Table 51. VBUS_SNK_DISCL
Address: 72h
Reset Value: 0xA0 (< vSafe5V: 4.0 V)
Type: Read/Write

Bit #	Name	R/W/C	Size (Bits)	VBUS SINK Disconnect Threshold Low (Note 36)
7:0	VBUS_SNK_DISC	R/W	8	**Bits 7:0 of Sink Disconnect threshold**

36. Accuracy is set for 50 mV LSB and Bit 0 is ignored.

Table 52. VBUS_SNK_DISCH
Address: 73h
Reset Value: 0x00
Type: Read/Write

Bit #	Name	R/W/C	Size (Bits)	VBUS SINK Disconnect Threshold High
7:2	Reserved	R	6	**Reserved: 000000b**
1:0	VBUS_SNK_DISC	R/W	2	**Bits 9:8 of Sink Disconnect threshold**

Table 53. VBUS_STOP_DISCL
Address: 74h
Reset Value: 0x1C (< vSafe0V: 700 mV)
Type: Read/Write

Bit #	Name	R/W/C	Size (Bits)	VBUS Stop Discharge Threshold Low (Note 37)
7:0	VBUS_VTH_LO	R/W	8	**Bits 7:0 of Stop Discharge threshold**

37. Accuracy is set for 50 mV LSB and Bit 0 is ignored.

Table 54. VBUS_STOP_DISCH

Address: 75h
Reset Value: 0x00
Type: Read/Write

Bit #	Name	R/W/C	Size (Bits)	VBUS Stop Discharge Threshold High
7:2	Reserved	R	6	Reserved: 000000b
1:0				

Table 59. VCONN_OCP

Add e : A0►·

Re et Va. e: 0x0F

T e: Read/W te

Bit #	Name	R/W/C	Size (Bits)	VCONN Current Limit Description (Note 40)
7:4				

Table 62. GPIO2_CFG (continued)
Address: A5h
Reset Value: 0x00
Type: Read/Write

Bit #

Table 66. SNK_FRSWAP

WQFN16 3x3, 0.5P
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