- Packaged in:
  - 14-lead WQFN (2.5 mm × 2.5 mm, 0.5 mm Pitch)

Applications

- Charging/Wall Adaptors
- Automotive Cigarette Adapters
- Laptops, Notebooks
- Power Adapters
-

PIN CONFIGURATION

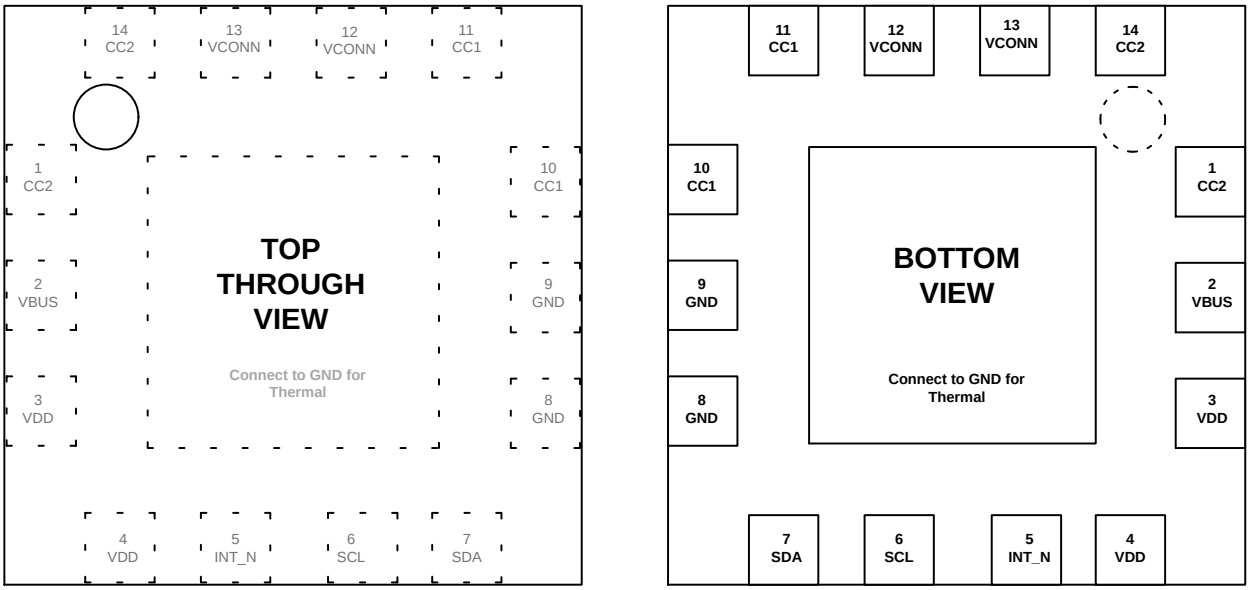


Figure 4. FUSB302TMPX Pin Assignment

Table 2. PIN DESCRIPTION

Name	Type	Description
USB TYPE-C CONNECTOR INTERFACE		
CC1/CC2	I/O	Type-C connector Configuration Channel (CC) pins. Initially used to determine when an attach has occurred and what the orientation of the insertion is. Functionality after attach depends on mode of operation detected. Operating as a host: 1. Sets the allowable charging current for VBUS to be sensed by the attached device 2. Used to communicate with devices using USB BMC Power Delivery 3. Used to detect when a detach has occurred Operating as a device: 1. Indicates what the allowable sink current is from the attached host. Used to communicate with devices using USB BMC Power Delivery
GND	Ground	Ground
VBUS	Input	VBUS input pin for attach and detach detection when operating as an upstream facing port (Device). Expected to be an OVP protected input.
POWER INTERFACE		
VDD	Power	Input supply voltage.
VCONN	Power Switch	Regulated input to be switched to correct CC pin as VCONN to power USB3.1 full-featured cables and other accessories.
SIGNAL INTERFACE		
SCL	Input	I^2C serial clock signal to be connected to the phone-based I^2C master.
SDA	Open-Drain I/O	I^2C serial data signal to be connected to the phone-based I^2C master
INT_N	Open-Drain Output	Active LOW open drain interrupt output used to prompt the processor to read the I^2C register bits

Table 3. PROCESSOR CONFIGURES THE FUSB302T THROUGH I^2C

I^2C Registers/Bits	Value
TOGGLE	1
PWR	07H
HOST_CUR0	1
HOST_CUR1	0

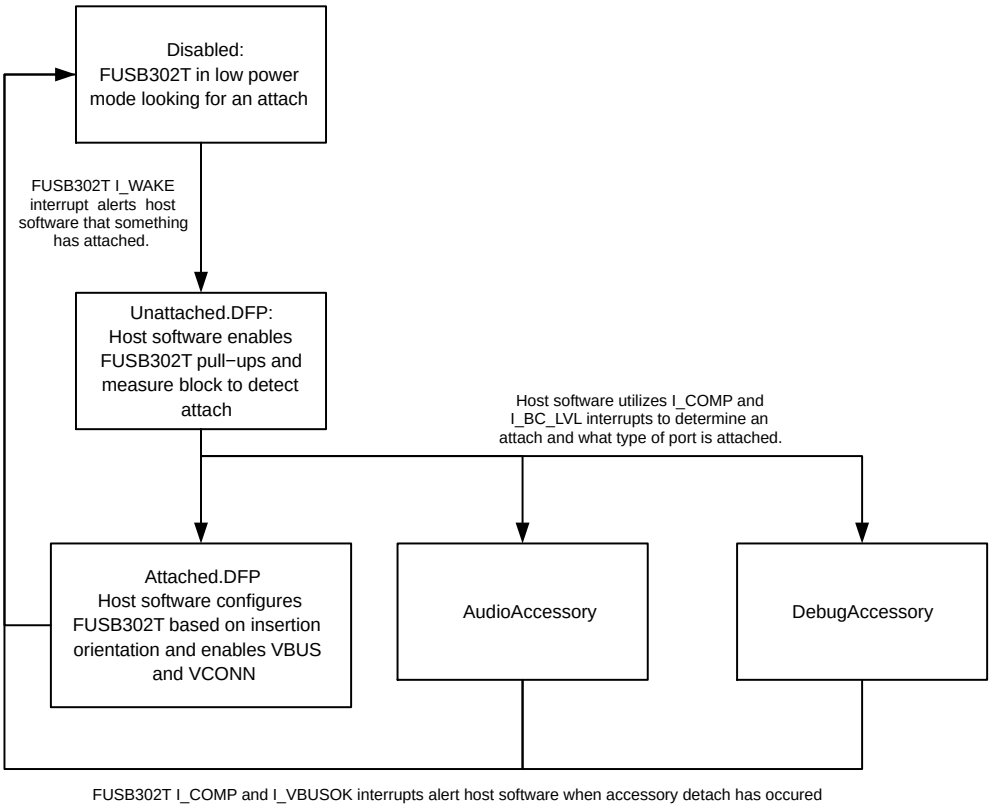


Figure 8. SRC Software Flow

Manual Dual-Role Detection and Configuration

The Type-C specification allows ports to be both a device and a host depending on what type of port has attached. This functionality is similar to USB OTG ports with the current USB connectors and is called a dual-role port. The FUSB302T can be used to implement a dual-role port. A Type-C dual role port toggles between presenting as a Type-C device and a Type-C host. The host software controls the toggle time and configuration of the FUSB302T in each state as shown in Figure 9.

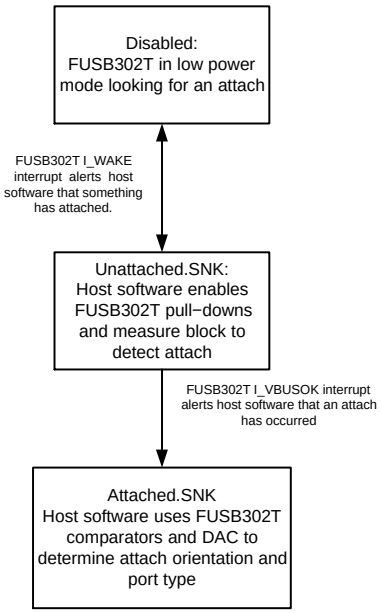


Figure 9. DRP Software Flow

BMC POWER DELIVERY

The Type-C connector allows USB Power Delivery (PD)

PD Send

The FUSB302T implements part of the PD protocol layer for sending packets in an autonomous fashion.

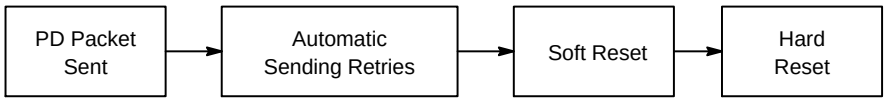


Figure 11.

PD Automatic Sending Retries

If GoodCRC packet is not received and AUTO_RETRY is set, then a retry of the same message that was in the TxFIFO written by the processor is executed within t_{Retry} and that is repeated for NRETRY times.

PD Send Soft Reset

If the correct GoodCRC packet is still not received for all retries then I_RETRYFAIL interrupt is triggered and if AUTO_SOFT_RESET is set, then a Soft Reset packet is created (MessageID is set to 0 and the processor upon servicing I_RETRYFAIL would set the true MessageIDCounter to 0.

If this Soft Reset is sent successfully where a GoodCRC control packet is received with a MessageID = 0 then I_TXSENT interrupt occurs.

If not, this Soft Reset packet is retried NRETRIES times (MessageID is always 0 for all retries) if a GoodCRC acknowledge packet is not received with CRCReceiveTimer expiring ($t_{Receive}$ of 1.1 ms max). If all retries fail, then I_SOFTFAIL interrupt is triggered.

PD Send Hard Reset

If all retries of the soft reset packet fail and if AUTO_HARD_RESET is set, then a hard reset ordered set is sent by loading up the TxFIFO with RESET1, RESET1, RESET1, RESET2 and sending a hard reset. Note only one hard reset is sent since the typical retry mechanism doesn't apply. The processor's policy engine firmware is responsible for retrying the hard reset if it doesn't receive the required response.

Flush Rx-FIFO with Built-In Self Test (BIST) Test Data

During PD compliance testing, BIST test packets are used to test physical layer of the PD interface such as, frequency derivation, Amplitude measure and etc. The one BIST test data packet has 7 data objects (28byte data), header and CRC, but the message ID doesn't change, the packet should be ignored and not acted on by the PD policy engine. The PD protocol layer does need to send a GoodCRC message back after every packet. The BIST data can arrive continuously from a tester, which could cause the FUSB302T Rx FIFO to overflow and the PD protocol layer to stop sending GoodCRC messages unless the FIFO is read or cleared quickly. The FUSB302T has a special register bit in the I^2C registers, bit[5] of address 0x09, that when the bit is set, all the data received next will be flushed from the RxFIFO automatically and the PD protocol layer will keep sending GoodCRC messages back. Once BIST test is done, tester sends HardReset, so with the HardReset, processor has to write the bit back to disable. Also, if the bit can be de-selected anytime, then the coming packet has to be managed by protocol layer and policy engine.

I^2C INTERFACE

The FUSB302T includes a full I^2C slave controller. The I^2C slave fully complies with the I^2C specification version 6 requieremnts. This block is designed for Fast Mode Plus traffic up to 1 MHz SCL operation.

The TOGGLE features allow for very low power operation with slow clocking thus may not be fully compliant to the 1 MHz operation. Examples of an I^2C write and read sequence are shown in Figure 12 and Figure 13 respectively.

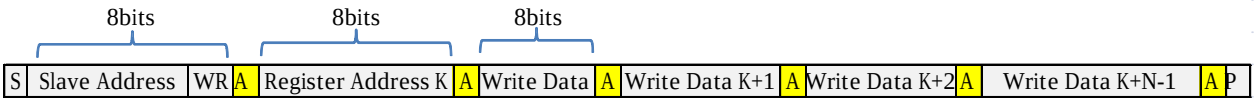


Figure 12. I^2C Write Example

[redacted]

				Max	Unit
				6.0	V
				6.0	V
V_{VBUS}	VBUS Supply Voltage		−0.5	28.0	V
$T_{STORAGE}$	Storage Temperature Range		−65	+150	°C
T_J	Maximum Junction Temperature		−	+150	°C
T_L	Lead Temperature (Soldering, 10 Seconds)		−	+260	°C
ESD	Human Body Model, ANSI/ESDA/JEDEC JS−001−2012	All Pins	4		

DC AND TRANSIENT CHARACTERISTICS

All typical values are at T_A = 25°C unless otherwise specified.

Table 8. BASEBAND PD

Symbol	Parameter	T_A = −40 to +85°C T_A = −40 to +105°C (Note 9) T_J = −40 to +125°C			Unit
		Min	Typ	Max	
UI	Unit Interval	3.03	−	3.70	μs
TRANSMITTER					
zDriver	Transmitter Output Impedance	33	−	75	Ω
$t_{EndDriveBMC}$	Time to Cease Driving the Line after the end of the last bit of the Frame	−	−	23	μs
$t_{HoldLowBMC}$					

Table 9. TYPE-C CC SWITCH

Symbol	Parameter	T_A = −40 to +85°C T_A = −40 to +105°C (Note 9) T_J = −40 to +125°C			Unit
		Min	Typ	Max	
R_{SW_CCx}	R_{DSON} for SW1_CC1 and SW1_CC2, VCONN to CC1 & CC2	−	0.4	1.2	Ω
I_{SW_CCX}	Over-Current Protection (OCP) limit at which VCONN switch shuts off over the entire VCONN voltage range (OCPreg = 0Fh)	600	800	1000	mA
tSoftStart	Time taken for the VCONN switch to turn on during which Over-Current Protection is disabled	−	1.5	−	ms
I_{80_CCX}	SRC 80 μA CC current (Default) HOST_CUR1 = 0, HOST_CUR0 = 1	64	80	96	μA
I_{180_CCX}	SRC 180 μA CC Current (1.5 A) HOST_CUR1 = 1, HOST_CUR0 = 0	166	180	194	μA
I_{330_CCX}	SRC 330 μA CC Current (3 A) HOST_CUR1 = 1, HOST_CUR0 = 1	304	330	356	μA
R_{DEVICE}	Device Pull-down Resistance (Note 6)	4.6	5.1	5.6	kΩ
zOPEN	CC Resistance for Disabled State	126	−	−	kΩ
$WAKE_{low}$	Wake threshold for CC pin SRC or SNK LOW value. Assumes bandgap and wake circuit turned on ie PWR[0] = 1	−	0.25	−	V
$WAKE_{high}$	Wake threshold for CC pin SRC or SNK HIGH value. Assumes bandgap and wake circuit turned on ie PWR[0] = 1	−	1.45	−	V
vBC_LVLhys	Hysteresis on the Ra and Rd Comparators (Note 8)	−	20	−	mV
vBC_LVL					

Table 10. CURRENT CONSUMPTION

Symbol	Parameter	V_{DD} (V)	Conditions	T_A = −40 to +85°C T_A = −40 to +105°C (Note 9) T_J = −40 to +125°C			Unit
				Min	Typ	Max	
Idisable	Disabled Current	3.0 to 5.5	Nothing Attached, No I^2C Transactions	−	0.37	5.0	μA
Itog	Unattached (standby) Toggle Current	3.0 to 5.5	Nothing attached, TOGGLE = 1, PWR[3:0] = 1h, WAKE_EN = 0, TOG_SAVE_PWR2:1 = 01	−	25	40	μA
Ipd_stby_meas	BMC PD Standby Current	3.0 to 5.5	Device Attached, BMC PD Active But Not Sending or Receiving Anything, PWR[3:0] = 7h	−	40	−	μA

Table 11. USB PD SPECIFIC PARAMETERS

Symbol	Parameter	T_A = −40 to +85°C T_A = −40 to +105°C (Note 9) T_J = −40 to +125°C			Unit
		Min	Typ	Max	
tHardReset	If a Soft Reset message fails, a Hard Reset is sent after tHardReset of CRCReceiveTimer expiring	−	−	5	ms
tHardReset Complete	If the FUSB302T cannot send a Hard Reset within tHardResetComplete time because of a busy line, then a I_HARDFAIL interrupt is triggered	−	−	5	ms
tReceive	This is the value for which the CRCReceiveTimer expires. The CRCReceiveTimer is started upon the last bit of the EOP of the transmitted packet	0.9	−	1.1	ms
tRetry	Once the CRCReceiveTimer expires, a retry packet has to be sent out within tRetry time. This time is hard to separate externally from tReceive since they both happen sequentially with no visible difference in the CC output	−	−	75	μs
tSoftReset	If a GoodCRC packet is not received within tReceive for NRETRIES then a Soft Reset packet is sent within tSoftReset time.	−	−	5	ms
tTransmit	From receiving a packet, we have to send a GoodCRC in response within tTransmit time. It is measured from the last bit of the EOP of the received packet to the first bit sent of the preamble of the GoodCRC packet	−	−	195	μs

Table 12. IO SPECIFICATIONS

Symbol	Parameter	V_{DD} (V)	Conditions	T_A = −40 to +85°C T_A = −40 to +105°C (Note 9) T_J = −40 to +125°C			Unit
				Min	Typ	Max	
HOST INTERFACE PINS (INT_N)							
V_{OLINTN}	Output Low Voltage	3.0 to 5.5	I_{OL} = 4 mA	−	−	0.4	V
T_{INT_Mask}	Time from global interrupt mask bit cleared to when INT_N goes LOW	3.0 to 5.5		50	−	−	μs
I^2C INTERFACE PINS – STANDARD, FAST, OR FAST MODE PLUS SPEED MODE (SDA, SCL) (Note 7)							
V_{ILI2C}	Low-Level Input Voltage	3.0 to 5.5		−	−	0.51	V
V_{IHI2C}	High-Level Input Voltage	3.0 to 5.5		1.32	−	−	V
V_{HYS}	Hysteresis of Schmitt Trigger Inputs	3.0 to 5.5		94	−	−	mV

Table 12. IO SPECIFICATIONS

Symbol	Parameter	V_{DD} (V)	Conditions	T_A = −40 to +85°C T_A = −40 to +105°C (Note 9) T_J = −40 to +125°C			Unit
				Min	Typ	Max	
I^2C INTERFACE PINS – STANDARD, FAST, OR FAST MODE PLUS SPEED MODE (SDA, SCL) (Note 7)							
I_{I2C}	Input Current of SDA and SCL Pins	3.0 to 5.5	Input Voltage 0.26 V to 2.0 V	−10	−	10	μA
I_{CCTI2C}	VDD Current when SDA or SCL is HIGH	3.0 to 5.5	Input Voltage 1.8 V	−10	−	10	μA
V_{OLSDA}	Low-Level Output Voltage (Open-Drain)	3.0 to 5.5	I_{OL} = 2 mA	0	−	0.35	V
I_{OLSDA}	Low-Level Output Current (Open-Drain)	3.0 to 5.5	V_{OLSDA} = 0.4 V	20	−	−	mA
C_I	Capacitance for Each I/O Pin (Note 8)	3.0 to 5.5		−	5	−	pF

7. I^2C pull up voltage is required to be between 1.71 V and V_{DD}.

Table 13. I^2C SPECIFICATIONS FAST MODE PLUS I^2C SPECIFICATIONS

Symbol	Parameter	Fast Mode Plus		Unit
		Min	Max	
f_{SCL}	I2C_SCL Clock Frequency	0	1000	kHz
$t_{HD;STA}$	Hold Time (Repeated) START Condition	0.26	−	μs
t_{LOW}	Low Period of I2C_SCL Clock	0.5	−	μs
t_{HIGH}	High Period of I2C_SCL Clock	0.26	−	μs
$t_{SU;STA}$	Set-up Time for Repeated START Condition	0.26	−	μs
$t_{HD;DAT}$	Data Hold Time	0	−	μs
$t_{SU;DAT}$	Data Set-up Time	50	−	ns
t_r	Rise Time of I2C_SDA and I2C_SCL Signals (Note 8)	−	120	ns
t_f	Fall Time of I2C_SDA and I2C_SCL Signals (Note 8)	6	120	ns
$t_{SU;STO}$	Set−up Time for STOP Condition	0.26	−	μs
t_{BUF}	Bus-Free Time between STOP and START Conditions (Note 8)	0.5	−	μs
t_{SP}	Pulse Width of Spikes that Must Be Suppressed by the Input Filter	0	50	ns
C_b	Capacitive Load for each Bus Line (Note 8)	−	550	pF
$t_{VD−DAT}$	Data Valid Time for Data from SCL LOW to SDA HIGH or LOW Output (Note 8)	0	0.45	μs
$t_{VD−ACK}$	Data Valid Time for acknowledge from SCL LOW to SDA HIGH or LOW Output (Note 8)	0	0.45	μs
V_{nL}	Noise Margin at the LOW Level (Note 8)	0.2	−	V
V_{nH}	Noise Margin at the HIGH Level (Note 8)	0.4	−	V

8. Guaranteed by Characterization and/or Design. Not production tested.
9. Automotive part only, FUSB302TVMPX, FUSB302TV01MPX, FUSB302TV10MPX, FUSB302TV11MPX

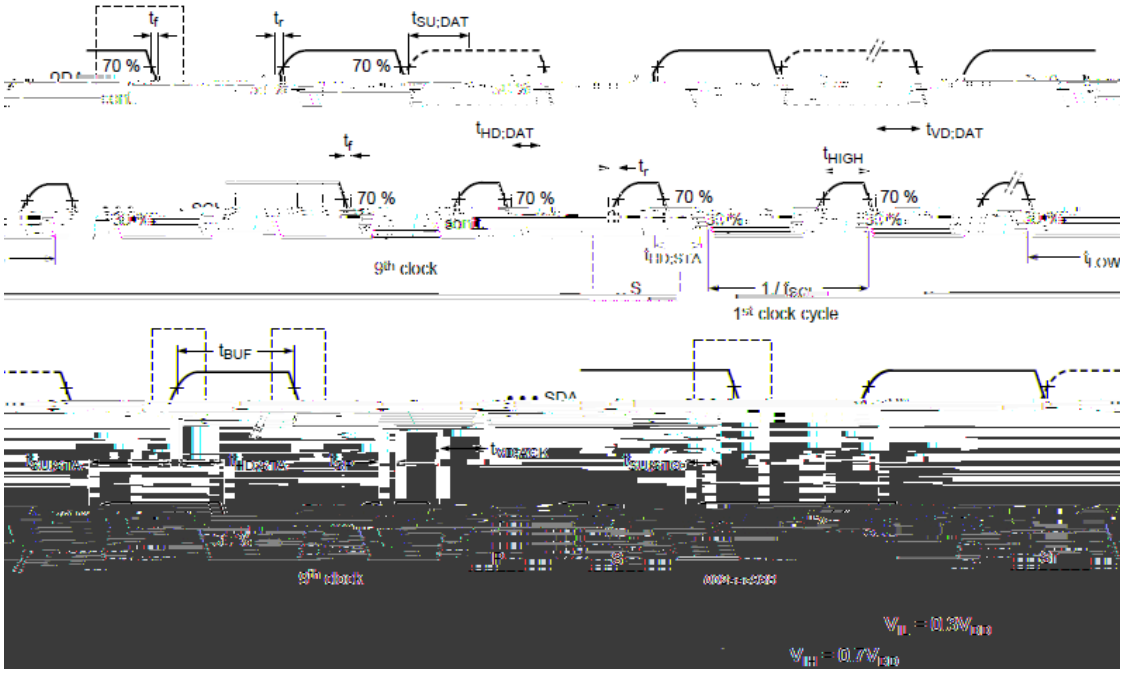

tF
tR
tSU;DAT
70 %
70 %
tHD;DAT
tVD;DAT
tHIGH
70 %
70 %
70 %
70 %
9th clock
tHD;STA
S
1 / fSCL
1st clock cycle
tLOW
tBUF
SDA
tSU;STA
tHD;STA
tWAKE:L
tSU;STO
9th clock
VIL = 0.3VDD
VIH = 0.7VDD

Table 15. REGISTER DEFINITIONS (Notes 10 and 11)

Address	Register Name	Type	Rst Val	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0B	Power	R/W	1					PWR3	PWR2	PWR1	PWR0
0x0C	Reset	W/C	0							PD_ RESET	SW_RES
0x0D											

Table 17. SWITCHES0

(Address: 02h; Reset Value: 0x0000_0000; Type: Read/Write)

Bit #	Name	R/W/C	Size (Bits)	Description
7	PU_EN2	R/W	1	1: Apply host pull up current to CC2 pin
6	PU_EN1	R/W	1	1: Apply host pull up current to CC1 pin
5	VCONN_CC2	R/W	1	1: Turn on the VCONN current to CC2 pin
4	VCONN_CC1	R/W	1	1: Turn on the VCONN current to CC1 pin
3	MEAS_CC2	R/W	1	1: Use the measure block to monitor or measure the voltage on CC2
2	MEAS_CC1	R/W	1	1: Use the measure block to monitor or measure the voltage on CC1
1	PDWN2	R/W	1	1: Device pull down on CC2. **0: No pull down**
0	PDWN1	R/W	1	1: Device pull down on CC1. **0: No pull down**

Table 18. SWITCHES1

(Address: 03h; Reset Value: 0x0010_0000; Type: Read/Write)

Bit #	Name	R/W/C	Size (Bits)	Description
7	POWERROLE	R/W	1	Bit used for constructing the GoodCRC acknowledge packet. This bit corresponds to the Port Power Role bit in the message header if an SOP packet is received: 1: Source if SOP **0: Sink if SOP**
6:5	SPECREV1: SPECREV0	R/W	2	Bit used for constructing the GoodCRC acknowledge packet. These bits correspond to the Specification Revision bits in the message header: 00: Revision 1.0 **01: Revision 2.0** 10: Do Not Use 11: Do Not Use
4	DATAROLE	R/W	1	Bit used for constructing the GoodCRC acknowledge packet. This bit corresponds to the Port Data Role bit in the message header. For SOP: 1: SRC **0: SNK**
3	Reserved	N/A	1	Do Not Use
2	AUTO_CRC	R/W	1	1: Starts the transmitter automatically when a message with a good CRC is received and automatically sends a GoodCRC acknowledge packet back to the relevant SOP* **0: Feature disabled**
1	TXCC2	R/W	1	1: Enable BMC transmit driver on CC2 pin
0	TXCC1	R/W	1	1: Enable BMC transmit driver on CC1 pin

FUSB302T

Table 24. CONTROL3
(Address: 09h; Reset Value: 0x0000_0110; Type: (see column below))

Bit #	Name	R/W/C	Size (Bits)	Description
7	Reserved	N/A	1	Do Not Use
6	SEND_HARD_RESET	W/C	1	1: Send a hard reset packet (highest priority) **0: Don't send a soft reset packet**
5	BIST_TMODE	R/W	1	1: BIST mode. Receive FIFO is cleared immediately after sending GoodCRC response **0: Normal operation, All packets are treated as usual**
4	AUTO_HARDRESET	R/W	1	1: Enable automatic hard reset packet if soft reset fail **0: Disable automatic hard reset packet if soft reset fail**
3	AUTO_SOFTRESET	R/W	1	1: Enable automatic soft reset packet if retries fail **0: Disable automatic soft reset packet if retries fail**
2:1	N_RETRIES[1:0]	R/W	2	**11: Three retries of packet (four total packets sent)** 10: Two retries of packet (three total packets sent) 01: One retry of packet (two total packets sent) 00: No retries (similar to disabling auto retry)
0	AUTO_RETRY	R/W	1	1: Enable automatic packet retries if GoodCRC is not received **0: Disable automatic packet retries if GoodCRC not received**

Table 25. MASK
(Address: 0Ah; Reset Value: 0x0000_0000; Type: Read/Write)

Bit #	Name	R/W/C	Size (Bits)	Description
7	M_VBUSOK	R/W	1	1: Mask I_VBUSOK interrupt bit **0: Do not mask**
6	M_ACTIVITY	R/W	1	1: Mask interrupt for a transition in CC bus activity **0: Do not mask**
5	M_COMP_CHNG	R/W	1	1: Mask I_COMP_CHNG interrupt for change is the value of COMP, the measure comparator **0: Do not mask**
4	M_CRC_CHK	R/W	1	1: Mask interrupt from CRC_CHK bit **0: Do not mask**
3	M_ALERT	R/W	1	1: Mask the I_ALERT interrupt bit **0: Do not mask**
2	M_WAKE	R/W	1	1: Mask the I_WAKE interrupt bit **0: Do not mask**
1	M_COLLISION	R/W	1	1: Mask the I_COLLISION interrupt bit **0: Do not mask**
0	M_BC_LVL	R/W	1	1: Mask a change in host requested current level **0: Do not mask**

Table 26. POWER
(Address: 0Bh; Reset Value: 0x0000_0001; Type: Read/Write)

Bit #	Name	R/W/C	Size (Bits)	Description
7:4	Reserved	N/A	4	Do Not Use
3:0	PWR[3:0]	R/W	4	Power enables: **PWR[0]: Bandgap and wake circuit** PWR[1]: Receiver powered and current references for Measure block PWR[2]: Measure block powered PWR[3]: Enable internal oscillator

3	OCP_RANGE	R/W	1	1: OCP range between 100−800 mA (max_range = 800 mA) 0: OCP range between 10−80 mA (max_range = 80 mA)
2:0	OCP_CUR2, OCP_CUR1, OCP_CUR0	R/W	3	111: max_range (see bit definition above for OCP_RANGE) 110: 7 × max_range / 8 101: 6 × max_range / 8 100: 5 × max_range / 8 011: 4 × max_range / 8 010: 3 × max_range / 8 001: 2 × max_range / 8 000: max_range / 8

Table 32. STATUS0A
(Address: 3Ch; Reset Value: 0x0000_0000; Type: Read)

Bit #	Name	R/W/C	Size (Bits)

Table 34. INTERRUPTA
(Address: 3Eh; Reset Value: 0x0000_0000; Type: Read/Clear)

Bit #	Name	R/W/C	Size (Bits)	Description
7	I_OCP_TEMP	R/C	1	1: Interrupt from either a OCP event on one of the VCONN switches or an over-temperature event
6	I_TOGDONE	R/C	1	1: Interrupt indicating the TOGGLE functionality was terminated because a device was detected
5	I_SOFTFAIL	R/C	1	1: Interrupt from automatic soft reset packets with retries have failed
4	I_RETRYFAIL	R/C	1	1: Interrupt from automatic packet retries have failed
3	I_HARDSENT	R/C	1	1: Interrupt from successfully sending a hard reset ordered set
2	I_TXSENT	R/C	1	1: Interrupt to alert that we sent a packet that was acknowledged with a GoodCRC response packet
1	I_SOFTRST	R/C	1	1: Received a soft reset packet
0	I_HARDRST	R/C	1	1: Received a hard reset ordered set

Table 35. INTERRUPTB
(Address: 3Fh; Reset Value: 0x0000_0000; Type: Read/Clear)

Bit #	Name	R/W/C	Size (Bits)	Description
7:1	Reserved	N/A	7	Do Not Use
0	I_GCRCSENT	R/C	1	1: Sent a GoodCRC acknowledge packet in response to an incoming packet that has the correct CRC value

Table 36. STATUS0
(Address: 40h; Reset Value: 0x0000_0000; Type: Read)

Bit #	Name	R/W/C	Size (Bits)	Description
7	VBUSOK	R	1	1: Interrupt occurs when VBUS transitions through vVBUSthr. This bit typically is used to recognize port partner during startup
6	ACTIVITY	R	1	1: Transitions are detected on the active CC* line. This bit goes high after a minimum of 3 CC transitions, and goes low with no Transitions **0: Inactive**
5	COMP	R	1	1: Measured CC* input is higher than reference level driven from the MDAC **0: Measured CC* input is lower than reference level driven from the MDAC**
4	CRC_CHK	R	1	1: Indicates the last received packet had the correct CRC. This bit remains set until the SOP of the next packet **0: Packet received for an enabled SOP* and CRC for the enabled packet received was incorrect**
3	ALERT	R	1	1: Alert software an error condition has occurred. An alert is caused by: TX_FULL: the transmit FIFO is full RX_FULL: the receive FIFO is full See **Status1** bits
2	WAKE	R	1	1: Voltage on CC indicated a device attempting to attach 0: WAKE either not enabled (WAKE_EN=0) or no device attached
1:0	BC_LVL[1:0]	R	2	Current voltage status of the measured CC pin interpreted as host current levels as follows: 00: < 200 mV 01: > 200 mV, < 660 mV 10: > 660 mV, < 1.23 V 11: > 1.23 V Note the software must measure these at an appropriate time, while there is no signaling activity on the selected CC line. BC_LVL is only defined when Measure block is on which is when register bits PWR[2]=1 and either MEAS_CC1=1 or MEAS_CC2=1

Table 37. STATUS1
(Address: 41h; Reset Value: 0x0010_1000; Type: Read)

Bit #	Name	R/W/C	Size (Bits)	Description
7	RXSOP2	R	1	1: Indicates the last packet placed in the RxFIFO is type SOP" (SOP double prime)
6	RXSOP1	R	1	1: Indicates the last packet placed in the RxFIFO is type SOP' (SOP prime)
5	RX_EMPTY	R	1	1: The receive FIFO is empty
4	RX_FULL	R	1	1: The receive FIFO is full
3	TX_EMPTY	R	1	1: The transmit FIFO is empty
2	TX_FULL	R	1	1: The transmit FIFO is full
1	OVRTEMP	R	1	1: Temperature of the device is too high
0	OCP	R	1	1: Indicates an over-current or short condition has occurred on the VCONN switch

Table 38. INTERRUPT

(Address: 42h; Reset Value: 0x0000_0000; Type: Read/Clear)

Bit #	Name	R/W/C	Size (Bits)	Description
7	I_VBUSOK	R/C	1	1: Interrupt occurs when VBUS transitions through 4.5 V. This bit typically is used to recognize port partner during startup
6	I_ACTIVITY	R/C	1	1: A change in the value of ACTIVITY of the CC bus has occurred
5	I_COMP_CHNG	R/C	1	1: A change in the value of COMP has occurred. Indicates selected CC line has tripped a threshold programmed into the MDAC
4	I_CRC_CHK	R/C	1	1: The value of CRC_CHK newly valid. I.e. The validity of the incoming packet has been checked

Table 40. TOKENS USED IN FIFO

Code	Name	Size (Bytes)	Description
101x−xxx1 (0xA1)	TXON	1	Alternative method for starting the transmitter with the TX−START bit. This is not a token written to the TxFIFO but a command much like TX_START but it is more convenient to write it while writing to the TxFIFO in one contiguous write operation. It is preferred that the TxFIFO is first written with data and then TXON or TX_START is executed. It is expected that A1h will be written for TXON not any other bits where x is non-zero such as B1h, BFh, etc
0x12	SOP1	1	When reaching the end of the FIFO causes a Sync−1 symbol to be transmitted
0x13	SOP2	1	When reaching the end of the FIFO causes a Sync−2 symbol to be transmitted
0x1B	SOP3	1	When reaching the end of the FIFO causes a Sync−3 symbol to be transmitted
0x15	RESET1	1	When reaching the end of the FIFO causes a RST−1 symbol to be transmitted
0x16	RESET2	1	When reaching the end of the FIFO causes a RST−2 symbol to be transmitted
0x80	PACKSYM	1+N	This data token must be immediately followed by a sequence of N packed data bytes. This token is defined by the 3 MSB's being set to 3'b100. The 5 LSB's are the number of packed bytes being sent. Note: N cannot be less than 2 since the minimum control packet has a header that is 2 bytes and N cannot be greater than 30 since the maximum data packet has 30 bytes (2 byte header + 7 data objects each having 4 bytes) Packed data bytes have two 4 bit data fields. The 4 LSB's are sent first, after 4b5b conversion etc in the chip
0xFF	JAM_CRC	1	Causes the CRC, calculated by the hardware, to be inserted into the transmit stream when this token reaches the end of the TX FIFO
0x140x14			

REFERENCE SCHEMATIC

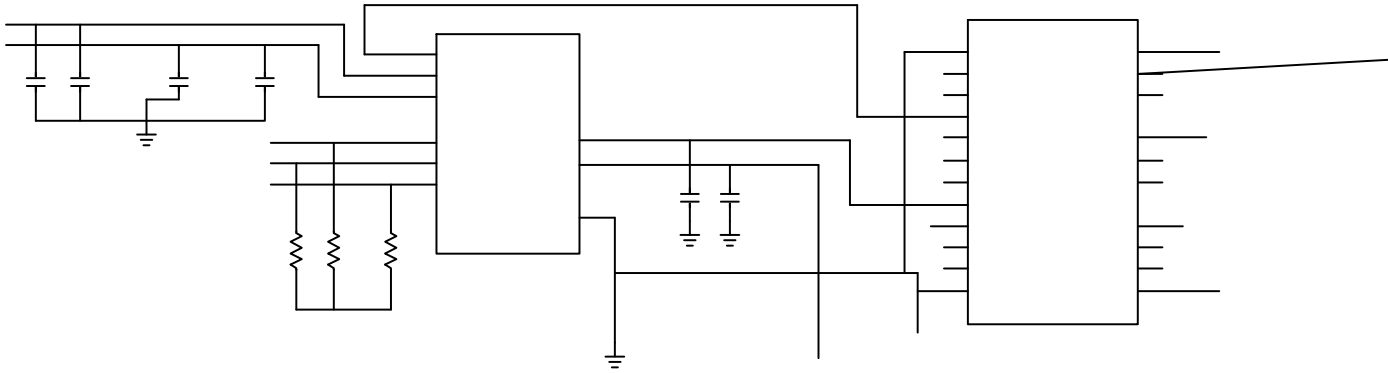
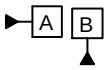


Figure 16. FUSB302T Reference Schematic Diagram

WQFN14 2.5x2.5, 0.5P
CASE 510BR
ISSUE O

DATE 31 AUG 2016



NOTES:

A. NO JEDEC REGISTRATION.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.

D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.

BOTTOM VIEW