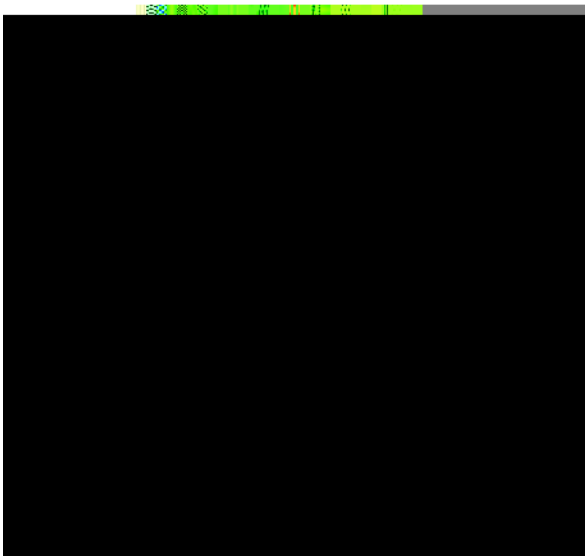
Is Now Part of



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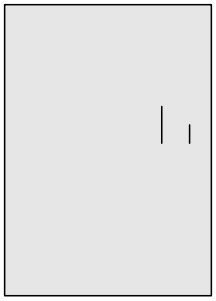
www.onsemi.com

Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

February 2013

Application Circuit Diagram



Pin Configuration

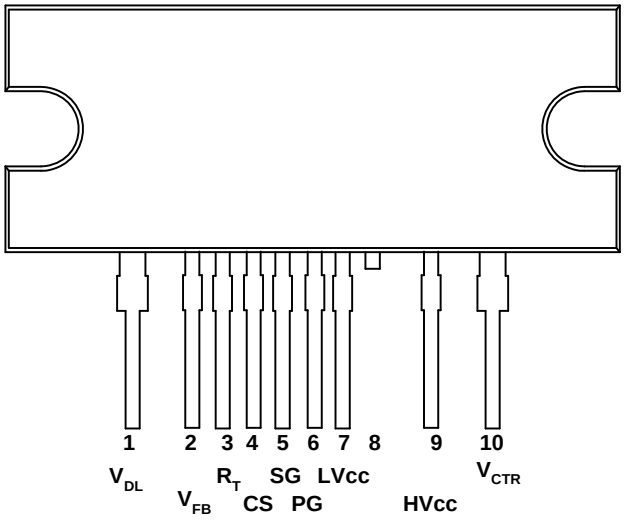


Figure 4. Package Diagram

Pin Definitions

Pin #	Name	Description
1	V_{DL}	This is the drain of the high-side MOSFET, typically connected to the input DC link voltage.
2	V_{FB}	This pin is connected to the inverting input of the PWM comparator internally and to the opto-coupler externally. The duty cycle is determined by the voltage on this pin.
3	R_T	

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. T_A=25°C unless otherwise specified.

Symbol	Parameter		Min.	Max.	Unit
V_{DS}	Maximum Drain-to-Source Voltage (V_{DL}-V_{CTR} and V_{CTR-PG})		600		V
LV_{CC}	Low-Side Supply Voltage		-0.3	25.0	V
HV_{CC} to V_{CTR}	High-Side V_{CC} Pin to Low-Side Drain Voltage		-0.3	25.0	V
HV_{CC}	High-Side Floating Supply Voltage		-0.3	625.0	V
V_{FB}	Feedback Pin Input Voltage		-0.3	LV_{CC}	V
V_{CS}	Current Sense (CS) Pin Input Voltage		-5.0	1.0	V
V_{RT}	R_T Pin Input Voltage		-0.3	5.0	V
dV_{CTR}/dt	Allowable Low-Side MOSFET Drain Voltage Slew Rate			50	V/ns
P_D	Total Power Dissipation[3]			12.0	W
T_J	Maximum Junction Temperature[4]			+150	°C
	Recommended Operating Junction Temperature[4]		-40	+130	
T_{STG}	Storage Temperature Range		-55	+150	°C
MOSFET Section					
V_{DGR}	Drain Gate Voltage (R_{GS}=1MΩ)		600		V
V_{GS}	Gate Source (GND) Voltage			±30	V
I_{DM}	Drain Current Pulsed			33	A
I_D	Continuous Drain Current	T_C=25°C		11	A
		T_C=100°C		7	
Package Section					
Torque	Recommended Screw Torque		5~7		kgf·cm

Notes:
3. Per MOSFET when both MOSFETs are conducting.
4. The maximum value of the recommended operating junction temperature is limited by thermal shutdown.

Thermal Impedance

T_A=25°C unless otherwise specified.

Symbol	Parameter	Value	Unit
θ_{JC}	Junction-to-Case Center Thermal Impedance (Both MOSFETs Conducting)	10.44	ºC/W
θ_{JA}	Junction-to-Ambient Thermal Impedance	80	ºC/W

Electrical Characteristics

T_A=25°C and LV_{CC}=17 V unless otherwise specified.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
MOSFET Section						
BV_{DSS}	Drain-to-Source Breakdown Voltage	I_D=200 µA, T_A=25°C	600			V
		I_D=200 µA, T_A=125°C		650		
$R_{DS(ON)}$	On-State Resistance	V_{GS}=10 V, I_D=5.5 A		0.32	0.38	Ω
t_{rr}	Body Diode Reverse Recovery Time[5]	V_{GS}=0 V, I_{Diode}=11.0 A, dI_{Diode}/dt=100 A/µs		120		ns
C_{ISS}	Input Capacitance[5]	V_{DS}=25 V, V_{GS}=0 V, f=1.0 MHz		1148		pF

Electrical Characteristics (Continued)

T_A=25°C and LV_{CC}=17 V unless otherwise specified.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Protection Section						
I_{OLP}	OLP Delay Current	V_{FB}=5 V	3.8	5.0	6.2	µA
V_{OLP}	OLP Protection Voltage	V_{FB} > 6 V	6.3	7.0	7.7	V
V_{OVP}	LV_{CC} Over-Voltage Protection	LV_{CC} > 21 V	21	23	25	V
V_{AOCP}	AOCP Threshold Voltage	ΔV/Δt=-1 V/µs	-1.0	-0.9	-0.8	V
t_{BAO}	AOCP Blanking Time(5)	V_{CS} < V_{AOCP}; ΔV/Δt=-1 V/µs		50		ns
t_{DA}	Delay Time (Low-Side) from V_{AOCP} to Switch Off(5)	ΔV/Δt=-1 V/µs		250	400	ns
V_{LIM}	Pulse-by-Pulse Current Limit Threshold Voltage	ΔV/Δt=-0.1 V/µs	-0.64	-0.58	-0.52	V
t_{BL}	Pulse-by-Pulse Current Limit Blanking Time	V_{CS} < V_{LIM}; ΔV/Δt=-0.1 V/µs		150		ns
t_{DL}	Delay Time (Low-Side) from V_{LIM} to Switch Off(5)	ΔV/Δt=-0.1 V/µs		450		ns
T_{SD}	Thermal Shutdown Temperature(5)		110	130	150	°C
I_{SU}	Protection Latch Sustain LV_{CC} Supply Current	LV_{CC}=7.5 V		100	150	µA
V_{PRSET}	Protection Latch Reset LV_{CC} Supply Voltage		5			V
Dead-Time Control Section						
D_T	Dead Time(6)			200		ns

Notes:
5. This parameter, although guaranteed, is not tested in production.
6. These parameters, although guaranteed, are tested only in EDS (wafer test) process.

Typical Performance Characteristics

These characteristic graphs are normalized at T_A=25°C.

Typical Performance Characteristics (Continued)

These characteristic graphs are normalized at T_A=25ºC.

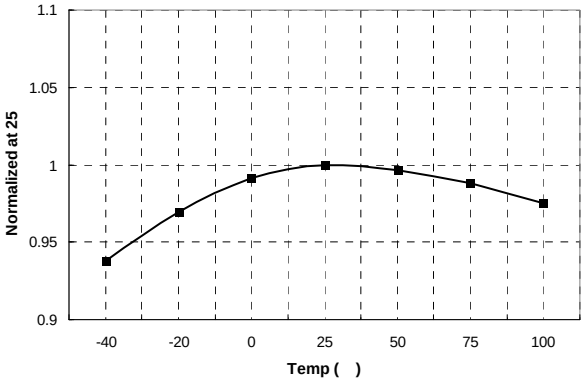


Figure 11. OLP Delay Current vs. Temperature

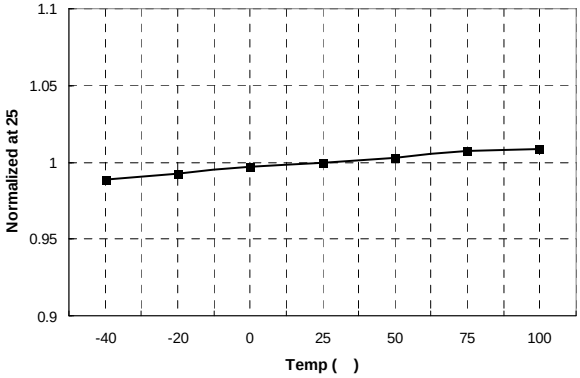


Figure 12. OLP Voltage vs. Temperature

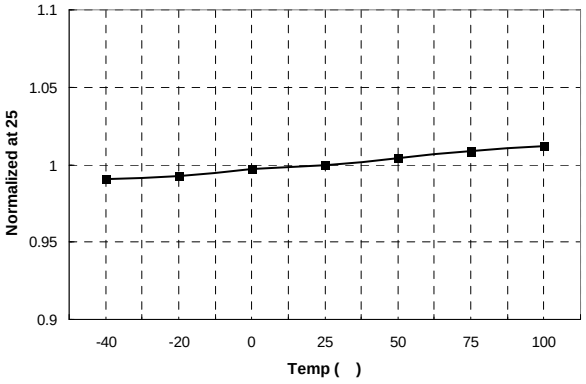


Figure 13. LV_{CC} OVP Voltage vs. Temperature

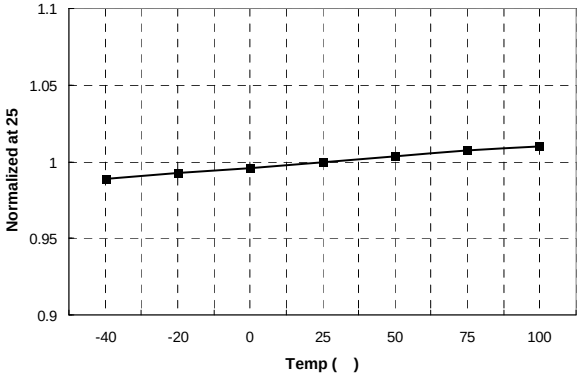


Figure 14. R_T Voltage vs. Temperature

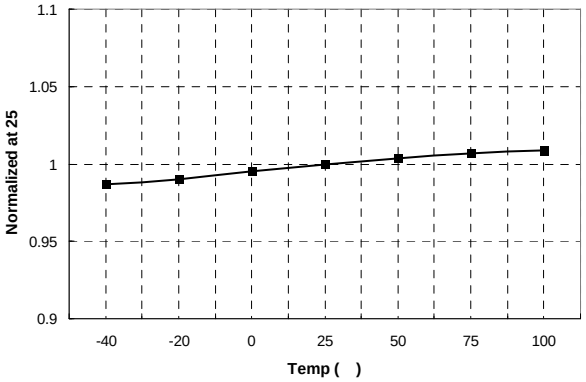


Figure 15. V_{BH} Voltage vs. Temperature

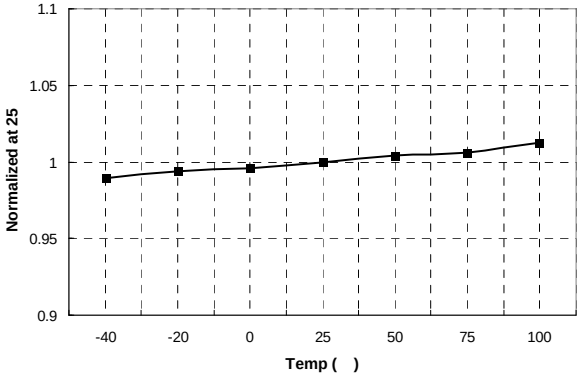
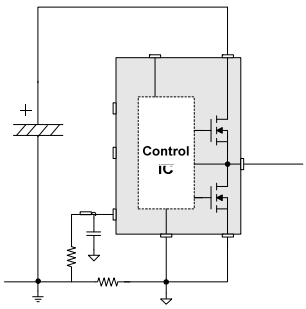


Figure 16. V_{LIM} Voltage vs. Temperature

Functional Description

1. Internal Oscillator: FSFA2100 employs a current-



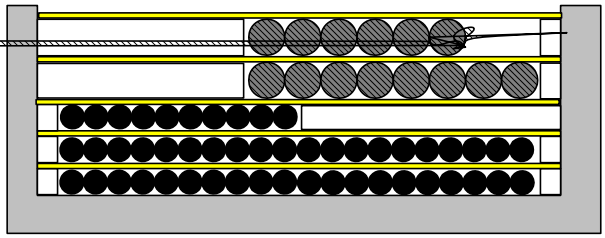
Typical Application Circuit (Asymmetric PWM Half-Bridge Converter)

Application	FPS™ Device	Input Voltage Range	Rated Output Power	Output Voltage (Rated Current)
LCD TV	FSFA2100	400 V	200 W	25 V-8 A

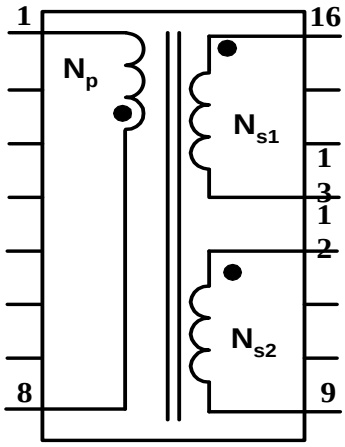
Features

Typical Application Circuit (Continued)

Core: EER3542 (Ae=107 mm^2)
Bobbin: EER3542 (Horizontal)



EER3542



26.20
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