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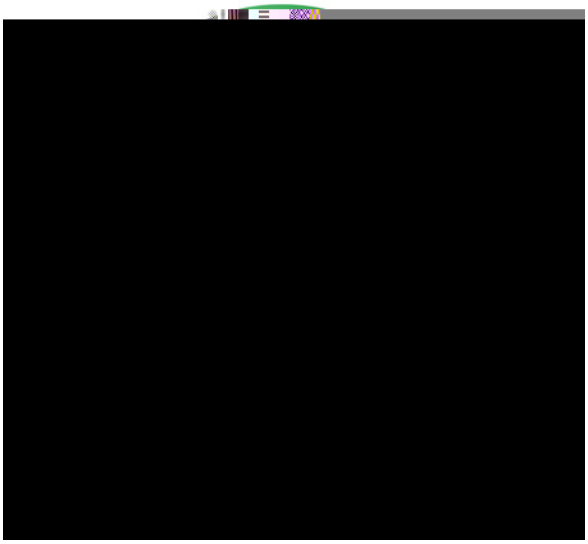

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Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

Internal Block Diagram

Figure 2. Functional Block Diagram of FSDM1265RB

Pin Definitions

Pin Number	Pin Name	Pin Function Description
1	Drain	This pin is the high voltage power Sense FET drain. It is designed to drive the transformer directly.
2	GND	This pin is the control ground and the Sense FET source.
3	Vcc	This pin is the positive supply voltage input. During startup, the power is supplied by an internal high voltage current source that is connected to the Vstr pin. When Vcc reaches 12V, the internal high voltage current source is disabled and the power is supplied from the auxiliary transformer winding.
4	Vfb	This pin is internally connected to the inverting input of the PWM comparator. The collector of an opto-coupler is typically tied to this pin. For stable operation, a capacitor should be placed between this pin and GND. Once the pin reaches 6.0V, the overload protection is activated resulting in the shutdown of the FPS^{TM}.
5	N.C	
6	Vstr	This pin is connected directly to the high voltage DC link. At startup, the internal high voltage current source supplies internal bias and charges the external capacitor that is connected to the Vcc pin. Once Vcc reaches 12V, the internal current source is disabled.cnn.3e(20.v60.92 r2753(t2C25TlV)97.9(a3V02a4P5412 016a/Tj1)97.042

Pin Configuration

Figure 3. Pin Configuration (Top View)

Absolute Maximum Ratings

(Ta=25°C, unless otherwise specified)

Parameter	Symbol	Value	Unit
Drain-source Voltage	V_{DSS}	650	V
Vstr Max. Voltage	V_{STR}	650	V
Pulsed Drain Current (Tc=25°C)(1)	I_{DM}	15.9	A_{DC}
Continuous Drain Current(Tc=25°C)	I_D	5.3	A
Continuous Drain Current(Tc=100°C)		3.4	A
Supply Voltage	V_{CC}	20	V
Input Voltage Range	V_{FB}	-0.3 to V_{CC}	V
Total Power Dissipation (Tc=25°C with Infinite Heat Sink)	P_D	50	W
Operating Junction Temperature	T_j	Internally limited	°C
Operating Ambient Temperature	T_A	-25 to +85	°C
Storage Temperature Range	T_{STG}	-55 to +150	°C
ESD Capability, HBM Model (All Pins except for Vstr and Vfb)	-	2.0 (GND-Vstr/Vfb=1.5kV)	kV
ESD Capability, Machine Model (All Pins except for Vstr and Vfb)	-	300 (GND-Vstr/Vfb=225V)	V

Notes:

1. Repetitive rating: Pulse width limited by maximum junction temperature

Thermal Impedance

Parameter	Symbol	Package	Value	Unit
Junction-to-Case Thermal	θ_{JC}(1)	TO-220F-6L	2.5	°C/W

Notes:

1. Infinite cooling condition - Refer to the SEMI G30-88.

Electrical Characteristics

(Ta = 25°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Sense FET SECTION						
Drain-source breakdown voltage	BV_{DSS}	V_{GS} = 0V, I_D = 250μA	650	-	-	V
Zero gate voltage drain current	I_{DSS}	V_{DS} = 650V, V_{GS} = 0V	-	-	500	μA
		V_{DS}= 520V V_{GS} = 0V, T_C = 125°C	-	-	500	μA
Static drain source on resistance	$R_{DS(ON)}$	V_{GS} = 10V, I_D = 2.5A	-	0.75	0.9	Ω
Output capacitance	C_{OSS}	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz	-	78	-	pF
Turn-on delay time	$T_{D(ON)}$	V_{DD}= 325V, I_D= 5A	-	42	-	ns
Rise time	T_R		-	106	-	
Turn-off delay time	$T_{D(OFF)}$		-	330	-	
Fall time	T_F		-	110	-	
CONTROL SECTION						
Initial frequency	F_{OSC}	V_{FB} = 3V	60	66	72	kHz
Voltage stability	F_{STABLE}	13V ≤ Vcc ≤ 18V	0	1	3	%
Temperature stability (1)	ΔF_{OSC}	-25°C ≤ Ta ≤ 85°C	0	±5	±10	%
Maximum duty cycle	D_{MAX}	-	77	82	87	%
Minimum duty cycle	D_{MIN}	-	-	-	0	%
Start threshold voltage	V_{START}	V_{FB}=GND	11	12	13	V
Stop threshold voltage	V_{STOP}	V_{FB}=GND	7	8	9	V
Feedback source current	I_{FB}	V_{FB}=GND	0.7	0.9	1.1	mA
Soft-start time	T_S	Vfb=3	-	10	15	ms
Leading edge blanking time	T_{LEB}	-	-	250	-	ns
BURST MODE SECTION						
Burst mode voltages(1)	V_{BURH}	Vcc=14V	0.3	0.38	0.46	V
	V_{BURL}	Vcc=14V	0.39	0.49	0.59	V

Electrical Characteristics (Continued)

(Ta = 25°C unless otherwise specified)

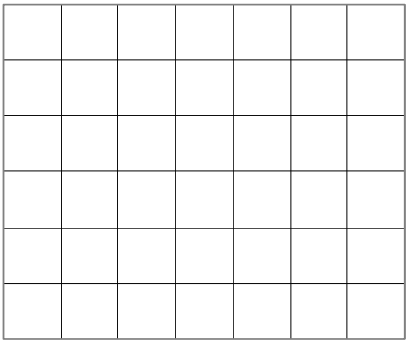
Notes:

Comparison of FS6M12653RTC and FSDM1265RB

Function	FS6M12653RTC	FSDM1265RB	FSDM1265RB Advantages
Soft-Start	Adjustable soft-start time using an external capacitor	Typical Internal soft-start of 10ms (fixed)	• Gradually increasing current limit during soft-start reduces peak current and voltage component stresses • Eliminates external components used for soft-start in most applications • Reduces or eliminates output overshoot
Burst Mode Operation	• Built into controller • Output voltage drops to about half	• Built into controller • Output voltage fixed	• Improves ight-load efficiency • Reduces no-load consumption

Typical Performance Characteristics (Continued)

(These Characteristic Graphs are Normalized at Ta= 25°C)



ShutDown Feedback Voltage vs. Temperature

ShutDown Delay Current vs. Temperature

Over Voltage Protection vs. Temperature

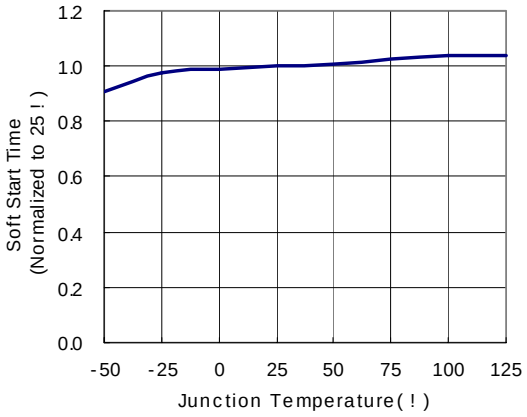
Current Limit VS. Temperature

Burst Mode Enable Voltage vs. Temperature

Burst Mode Disable Voltage vs. Temperature

Typical Performance Characteristics (Continued)

(These Characteristic Graphs are Normalized at Ta= 25°C)



Soft-start Time vs. Temperature

Functional Description

1. Star-tup: In previous generations of Fairchild Power Switches (FPS^{TM}), the Vcc pin had an external start-up to the DC input voltage line. In the newer switches, the startup resistor is replaced by an internal high voltage current source. At startup, an internal high voltage current source supplies the internal bias and charges the external capacitor (C_{VCC}) that is connected to the Vcc pin as illustrated in Figure 4. When the Vcc pin reaches 12V, the FSDM1265RB begins switching and the internal high voltage current source is disabled. Then, the FSDM1265RB continues its normal switching operation and the power is supplied from the auxiliary transformer winding unless Vcc goes below the stop voltage of 8V.

Figure 4. Internal startup circuit

2. Feedback Control: FSDM1265RB employs current mode control, as shown in Figure 5. An opto-coupler (such as the H11A817A) and shunt regulator (such as the KA431) are typically used to implement the feedback network. Comparing the feedback voltage with the voltage across the Rsense resistor in addition to the offset voltage makes it possible to control the switching duty cycle. When the reference pin voltage

Figure 6. Auto Restart Operation

3.1 Over Load Protection (OLP): Overload occurs when the load current exceeds a pre-set level due to an unexpected event. The protection circuit (OLP) is activated to protect the SMPS. However, even when the SMPS is operating normally, the OLP circuit can become activate during the load transition. To avoid this undesired operation, the OLP circuit is designed to become activate after a specified time to determine whether it is in a transient or an overload mode. Because of the pulse-by-pulse current limit capability, the maximum peak current through the SenseFET is limited, and therefore the maximum input power is restricted with a given input voltage. If the output consumes beyond this maximum power, the output voltage (Vo) decreases below the set voltage. This reduces the current through the opto-coupler LED, which also reduces the opto-coupler transistor current, thus increasing the feedback voltage

(Vfb). If Vfb exceeds 2.5V, D1 is blocked and the 3.5uA current source slowly starts to charge C_B up to Vcc. In this condition, Vfb continues increasing until it reaches 6V. Then the switching operation terminates as shown in Figure 7. The delay time for shutdown is the time required to charge C_B

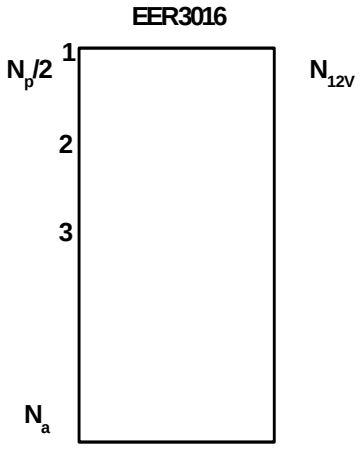
in Figure 8, the device automatically enters burst mode when the feedback voltage drops below V_{BURL}(380mV). At this point switching stops and the output voltages start to drop at a rate dependent on the standby current load. This causes

Typical Application Circuit

Features

- High efficiency (>81% at 85Vac input)
- Low zero-load power consumption (<300mW at 240Vac input)
- Low standby-mode power consumption (<800mW at 240Vac input and 0.3W load)
- Low component count
- Enhanced system reliability through several protection functions

2. Transformer Schematic Diagram



3.Winding Specification

No	Pin (s→f)	Wire	Turns	Winding Method
Na	4 → 5	$0.2^{\phi} \times 1$	8	Center Winding
Insulation: Polyester Tape t = 0.050mm, 2Layers				
Np/2	2 → 1	$0.4^{\phi} \times 1$	18	Solenoid Winding
Insulation: Polyester Tape t = 0.050mm, 2Layers				
N_{12V}	10 → 8	$0.3^{\phi} \times 3$	7	Center Winding
Insulation: Polyester Tape t = 0.050mm, 2Layers				
N5V	7 → 6	$0.3^{\phi} \times 3$	3	Center Winding
Insulation: Polyester Tape t = 0.050mm, 2Layers				
Np/2	3 → 2	$0.4^{\phi} \times 1$	18	Solenoid Winding
Outer Insulation: Polyester Tape t = 0.050mm, 2Layers				

4.Electrical Characteristics

	Pin	Specifications	Remarks
Inductance	1 - 3	420uH ± 10%	100kHz, 1V
Leakage Inductance	1 - 3	10uH Max.	2^{nd} all short

5. Core & Bobbin

Core: EER 3016
Bobbin: EER3016
Ae(mm2): 96

7. Layout

Figure 9. Layout Considerations for FSDM1265RB

Package Dimensions

NOTES: UNLESS OTHER

Ordering Information

Product Number	Package	Marking Code	BVdss	Rds(on)Max
FSDM1265RBWDTU	TO-220F-6L(Forming)	DM1265RB	650V	0.9 Ω

WDTu: Forming Type