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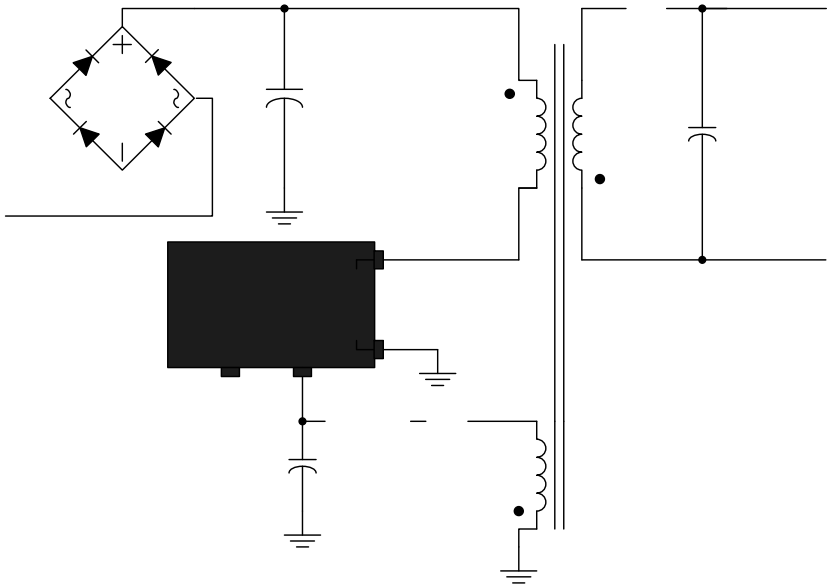
October 2011

FSD156MRBN — Green-Mode Fairchild Power Switch (FPS™)

Application Circuit



Pin Configuration

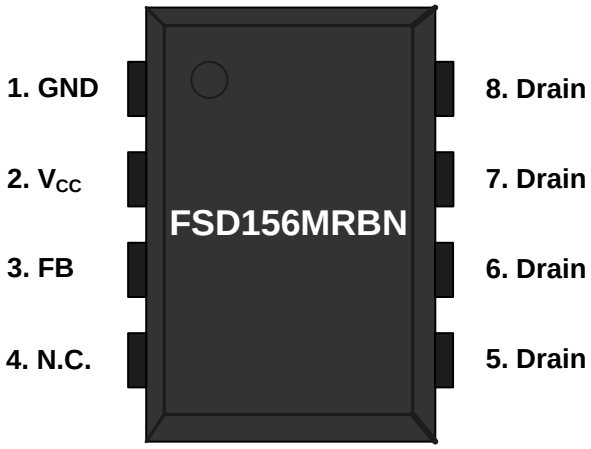


Figure 3. Pin Configuration (Top View)

Pin Definitions

Pin #	Name	Description

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{DS}	Drain Pin Voltage			650	V
V_{CC}	V_{CC} Pin Voltage			26	V
V_{FB}	Feedback Pin Voltage		-0.3	10.0	V
I_{DM}	Drain Current Pulsed			4	A
I_{DS}	Continuous Switching Drain Current[6]	T_C=25 C		1.9	A
		T_C=100 C		1.27	A
E_{AS}	Single Pulsed Avalanche Energy[7]			190	mJ
P_D	Total Power Dissipation (T_C=25 C)[8]			1.5	W
T_J	Maximum Junction Temperature			150	C
	Operating Junction Temperature[9]		-40	+125	C
T_{STG}	Storage Temperature		-55	+150	C
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22-A114		5	kV
		Charged Device Model, JESD22-C101		2	

Notes:

6. Repetitive peak switching current when the inductive load is assumed: Limited by maximum duty (D_{MAX}=0.73)

Electrical Characteristics

T_J = 25 C unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
SenseFET Section						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{CC} = 0V, I_D = 250 A	650			V
I_{DSS}	Zero-Gate-Voltage Drain Current	V_{DS} = 650V, T_A = 25 C			250	A
$R_{DS(ON)}$	Drain-Source On-State Resistance	V_{GS}=10V, I_D =1A		1.8	2.2	Ω
C_{ISS}	Input Capacitance[12]	V_{DS} = 25V, V_{GS} = 0V, f=1MHz		515		pF
C_{OSS}	Output Capacitance[12]	V_{DS} = 25V, V_{GS} = 0V, f=1MHz		75		pF
t_r	Rise Time	V_{DS} = 325V, I_D = 4A, R_G=25Ω		26		ns
t_f	Fall Time	V_{DS} = 325V, I_D = 4A, R_G=25Ω		25		ns
$t_{d(on)}$	Turn-On Delay	V_{DS} = 325V, I_D = 4A, R_G=25Ω		14		ns
$t_{d(off)}$	Turn-Off Delay	V_{DS} = 325V, I_D= 4A, R_G=25Ω		32		ns
Control Section						
f_S	Switching Frequency[12]	V_{CC} = 14V, V_{FB} = 4V	61	67	73	kHz
f_S	Switching Frequency Variation[12]	-25 C < T_J < 125 C		±5	±10	%
D_{MAX}	Maximum Duty Ratio	V_{CC} = 14V, V_{FB} = 4V	61	67	73	%
D_{MIN}	Minimum Duty Ratio	V_{CC} = 14V, V_{FB} = 0V			0	%
I_{FB}	Feedback Source Current	V_{FB} = 0	65	90	115	A
V_{START}	UVLO Threshold Voltage	V_{FB} = 0V, V_{CC}				

Electrical Characteristics (Continued)

T_J

Typical Performance Characteristics

Characteristic graphs are normalized at T_A=25°C.

Typical Performance Characteristics

Characteristic graphs are normalized at T_A

Functional Description

4. Protection Circuits: The FSD156MRBN has several self-protective functions, such as Overload Protection (OLP), Abnormal Over-Current Protection (AOCP), Output-Short Protection (OSP), Over-Voltage Protection (OVP), and Thermal Shutdown (TSD). All the protections are implemented as auto-restart. Once the fault condition is detected, switching is terminated and the SenseFET remains off. This causes V_{CC} to fall. When V_{CC} falls to the Under-Voltage Lockout (UVLO) stop voltage of 7.5V, the protection is reset and the startup circuit charges the V_{CC} capacitor. When V_{CC} reaches the start voltage of 12.0V, the FSD156MRBN resumes normal operation. If the fault condition is not removed, the SenseFET remains off and V_{CC} drops to

4.3. Output-Short Protection (OSP): If the output is shorted, steep current with extremely high di/dt can flow through the SenseFET during the minimum turn-on time. Such a steep current brings high-voltage stress on the drain of the SenseFET when turned off. To protect the device from this abnormal condition, OSP is included. It is comprised of detecting V_{FB} and SenseFET turn-on time. When the V_{FB} is higher than 2.0V and the SenseFET turn-on time is lower than 1.0μs, this condition is recognized as an abnormal error and PWM switching shuts down until V_{CC} reaches V_{START} again. An abnormal condition output short is shown in Figure 22.

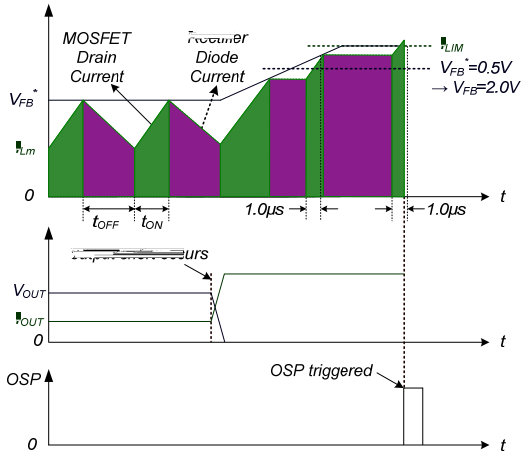


Figure 22. Output-Short Protection

4.4 Over-Voltage Protection (OVP): If the secondary-side feedback circuit malfunctions or a solder defect causes an opening in the feedback path, the current through the opto-coupler transistor becomes almost zero. Then V_{FB} climbs up in a similar manner to the overload situation, forcing the preset maximum current to be supplied to the SMPS until the overload protection is triggered. Because more energy than required is provided to the output, the output voltage may exceed the rated voltage before

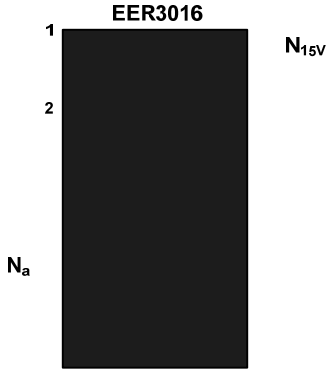
Typical Application Circuit

Application	Input Voltage	Rated Output	Rated Power
LCD Monitor Power Supply	85 ~ 265V_{AC}	5.0V(2A) 14.0V(1.3A)	28.2W

Key Design Notes

1. The delay for overload protection is designed to be about 30ms with C105 (8.2nF). OLP time between 39ms (12nF) and 46ms (15nF) is recommended.
2. The SMD-type capacitor (C106) must be placed as close as possible to the V_{CC} pin to avoid malfunction by

Transformer



Bill of Materials

Part #	Value	Note	Part #	Value	Note
Fuse			**Capacitor**		
F101	250V 2A		C101	220nF/275V	Box (Pilkor)
NTC			C102	150nF/275V	Box (Pilkor)
NTC101	5D-9	DSC	C103	100 F/400V	Electrolytic (SamYoung)
Resistor			C104	3.3nF/630V	Film (Sehwa)
R101	1.5MΩ, J	1W	C105	15nF/100V	Film (Sehwa)
R103	43kΩ, J	1W	C106	100nF	SMD (2012)
R201	1.5kΩ, F	1/4W, 1%	C107	47 F/50V	Electrolytic (SamYoung)
R202	1.0kΩ, F	1/4W, 1%	C201	820 F/25V	Electrolytic (SamYoung)