

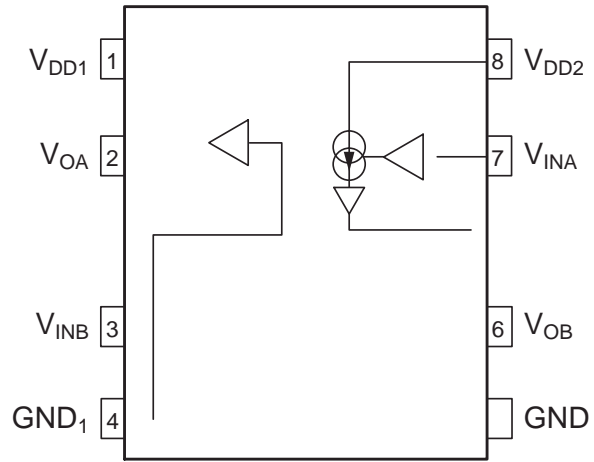
FOD8012A

TRUTH TABLE

V_{IN}	LED	V_O
High	OFF	High
Low	ON	Low

NOTE: When not communicating, V_{IN} must be in static high logic condition.

Functional Schematic



0.1 μ F bypass capacitor required from V_{DD} to GND

Figure 1. Functional Schematic

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ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise specified)

Symbol	Parameter	Value	Units
T _{STG}	Storage Temperature	-40 to +125	°

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SWITCHING CHARACTERISTICS (T_A = -40°C to +110°C, 3.0 V ≤ V_{DD} ≤ 5.5 V, unless otherwise specified.

Apply over all recommended conditions, typical value is measured at V_{DD1} = V_{DD2} = +3.3 V, T_A = 25°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
	Data Rate				15	Mbit/s
t _{PHL}	Propagation Delay Time to Logic Low Output	PW = 66.7 ns, C _L = 15 pF		37	60	ns
t _{PLH}	Propagation Delay Time to Logic High Output	PW = 66.7 ns, C _L = 15 pF		40	60	ns
PWD	Pulse Width Distortion, t _{PHL} - t _{PLH}	PW = 66.7 ns, C _L = 15 pF (Note 5)		3	15	ns
t _{PSK(CC)}	Channel-Channel Skew	PW = 66.7 ns, C _L = 15 pF (Note 6)		12	25	ns
t _{PSK(PP)}	Part-Part Skew	PW = 66.7 ns, C _L = 15 pF (Note 7)			30	ns
t _R	Output Rise Time (10% to 90%)	PW = 66.7 ns, C _L = 15 pF		6.5		ns
t _F	Output Fall Time (90% to 10%)	PW = 66.7 ns, C _L = 15 pF				ns



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TEST CIRCUITS

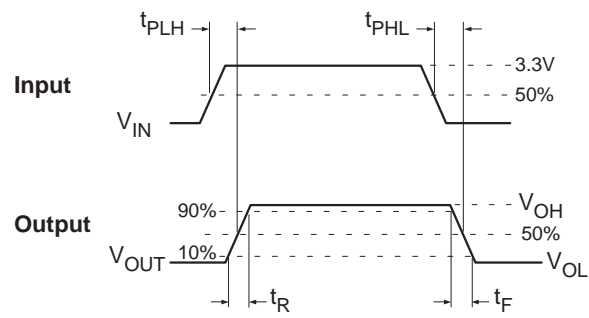
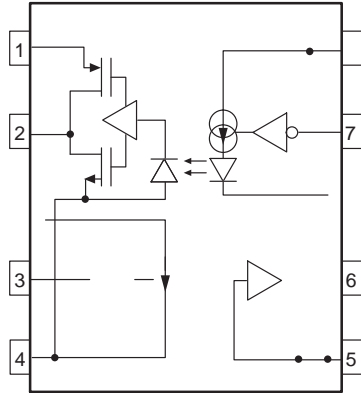


Figure 15. Test Circuit for Propagation Delay Time and Rise Time, Fall Time

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ALL DIMENSIONS

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