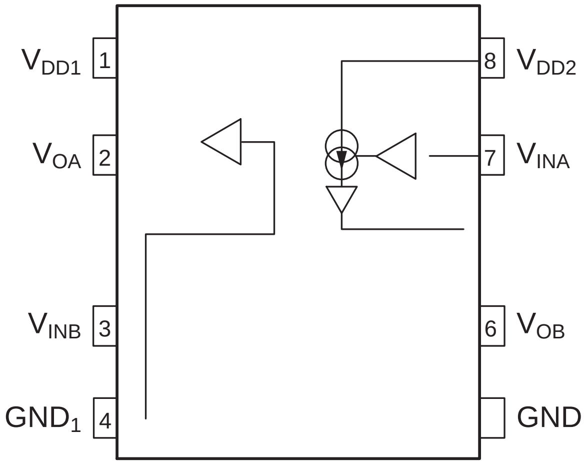
nse

TRUTH TABLE

V_{IN}	LED	V_O
High	OFF	High
Low	ON	Low

NOTE: When not communicating, V_{IN} must be in static high logic condition.

Functional Schematic



0.1µF bypass capacitor required from V_{DD} to GND

Figure 1. Functional Schematic

ABSOLUTE MAXIMUM RATINGS (T$_A$ = 25°C unless otherwise specified)

Symbol	Parameter	Value	Units
T_{STG}	Storage Temperature	−40 to +125	°

SWITCHING CHARACTERISTICS (T_A = −40°C to +110°C, 3.0 V ≤ V_{DD} ≤ 5.5 V, unless otherwise specified. Apply over all recommended conditions, typical value is measured at V_{DD1} = V_{DD2} = +3.3 V, T_A = 25°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
	Data Rate				15	Mbit/s
t_{PHL}	Propagation Delay Time to Logic Low Output	PW = 66.7 ns, C_L = 15 pF		37	60	ns
t_{PLH}	Propagation Delay Time to Logic High Output	PW = 66.7 ns, C_L = 15 pF		40	60	ns
PWD	Pulse Width Distortion, | t_{PHL} – t_{PLH} |	PW = 66.7 ns, C_L = 15 pF (Note 5)		3	15	ns
$t_{PSK(CC)}$	Channel−Channel Skew	PW = 66.7 ns, C_L = 15 pF (Note 6)		12	25	ns
$t_{PSK(PP)}$	Part−Part Skew	PW = 66.7 ns, C_L = 15 pF (Note 7)		[redacted]	30	ns
t_R	Output Rise Time (10% to 90%)	PW = 66.7 ns, C_L = 15 pF		6.5		ns
t_F	Output Fall Time (90% to 10%)	PW = 66.7 ns, C_L = 15 pF				

L55.6808413q514.43iof437.443 582.123 38.20 0 8 450.6519 572.8252 Tm(6.5)TjE513.921 5.c

[redacted]

TEST CIRCUITS

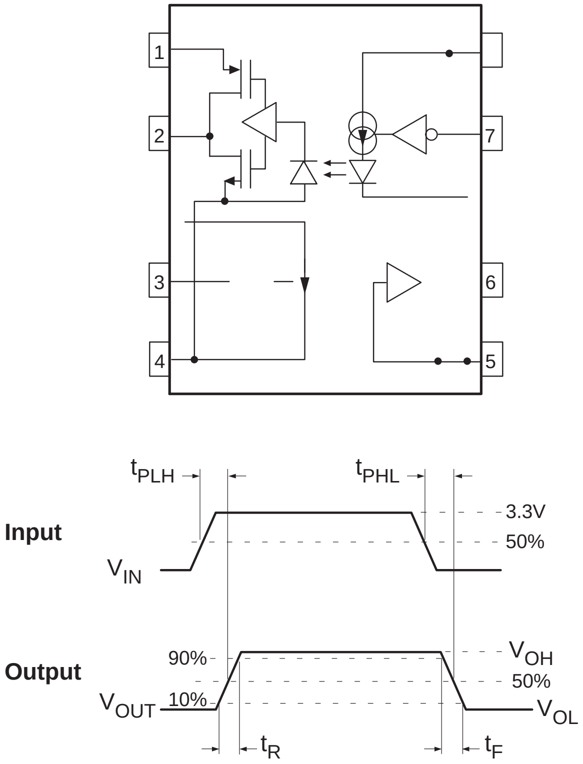


Figure 15. Test Circuit for Propagation Delay Time and Rise Time, Fall Time

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ALL DIMENSIONS