Schematics

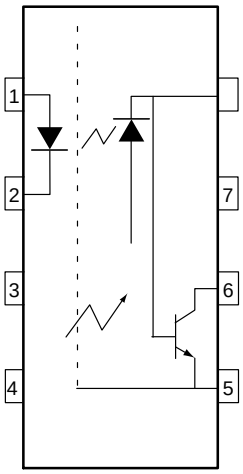


Figure 1. Schematics

ABSOLUTE MAXIMUM RATINGS (T_A = 25°

ELECTRICAL CHARACTERISTICS (Continued)
(T_A = 0°C to 70°C, unless otherwise specified.)

SWITCHING CHARACTERISTICS (V_{CC} = 3.3 V & 5 V)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
T_{PHL}	Propagation Delay Time to Logic LOW	R_L = 1.9 kΩ, I_F = 16 mA (Note 3)	25°C			1.0	μs
		(Figure 10)				2.0	
T_{PLH}	Propagation Delay Time to Logic HIGH	R_L = 1.9 kΩ, I_F = 16 mA (Note 3)	25°C			1.0	μs
		(Figure 10)				2.0	
$\|CM_H\|$	Common Mode Transient Immunity at Logic HIGH	I_F = 0 mA, V_{CM} = 1,000 V_{P-P}, R_L = 4.1 kΩ, T_A = 25°C (Notes 4, 5) (Figure 11)		5,000	50,000		V/μs
		I_F = 0 mA, V_{CM} = 1,000 V_{P-P}, R_L = 1.9 kΩ, T_A = 25°C (Notes 3, 5) (Figure 11)		5,000	50,000		V/μs
$\|CM_L\|$	Common Mode Transient Immunity at Logic LOW	I_F = 16 mA, V_{CM} = 1,000V_{P-P}, R_L = 4.1 kΩ, T_A = 25°C (Notes 4, 5) (Figure 11)		5,000	35,000		V/μs
		I_F = 16 mA, V_{CM} = 1,000 V_{P-P}, R_L = 1.9 kΩ, T_A = 25°C (Notes 3, 5) (Figure 11)		5,000	35,000		V/μs

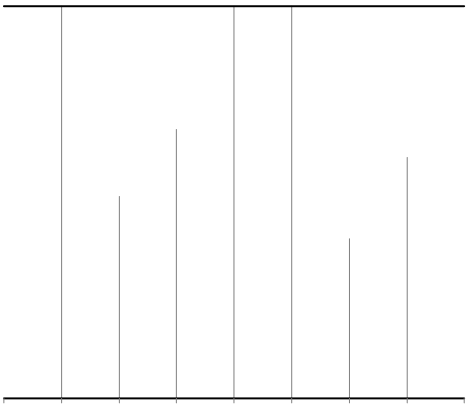
ISOLATION CHARACTERISTICS

Symbol	Characteristics	Test Conditions	Min.	Typ.	Max.	Unit
I_{I-O}	Input−Output Insulation Leakage Current	Relative humidity = 45%, T_A = 25°C, t = 5 s, V_{I-O} = 3000 VDC (Note 6)			1.0	μA
V_{ISO}	Withstand Insulation Test Voltage	f = 60 Hz, T_A = 25°C, t = 60 s (Note 6)	2500			V_{RMS}
R_{I-O}	Resistance (Input to Output)	V_{I-O} = 500 VDC (Note 6)	10^{11}	10^{12}		Ω
C_{I-O}	Capacitance (Input to Output)	f = 1 MHz (Note 6)		0.2		pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. The 1.9 kΩ load represents 1 TTL unit load of 1.6 mA and 5.6 kΩ pull−up resistor.
4. The 4.1 kΩ load represents 1 LSTTL unit load of 0.36 mA and 6.1 kΩ pull−up resistor.
5. Common mode transient immunity in logic high level is the maximum tolerable (positive) dV_{cm} / dt on the leading edge of the common mode pulse signal V_{CM}, to assure that the output will remain in a logic high state (i.e., V_O > 2.0 V). Common mode transient immunity in logic low level is the maximum tolerable (negative) dV_{cm} / dt on the trailing edge of the common mode pulse signal, V_{CM}, to assure that the output will remain in a logic low state (i.e., V_O < 0.8 V).
6. Device is considered a two terminal device: pins 1, 2, 3 and 4 are shorted together and pins 5, 6, 7 and 8 are shorted together.

TYPICAL PERFORMANCE CURVES



V_F – FORWARD VOLTAGE (V)mA0 G.73158.4 5791.168 T 0 0 m281

Figure 2. LED Forward Current vs. Forward Voltage

Figure 3. Current Transfer Ratio vs. Forward Current

Figure 4. Current Transfer Ratio vs. Ambient Temperature

Figure 5. Output Current vs. Output Voltage

Figure 6. Logic High Output Current vs. Ambient Temperature

Figure 7. Supply Current vs. Input Forward Current

TEST CIRCUITS

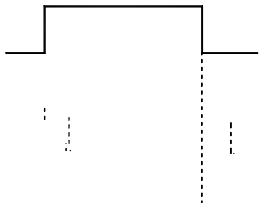
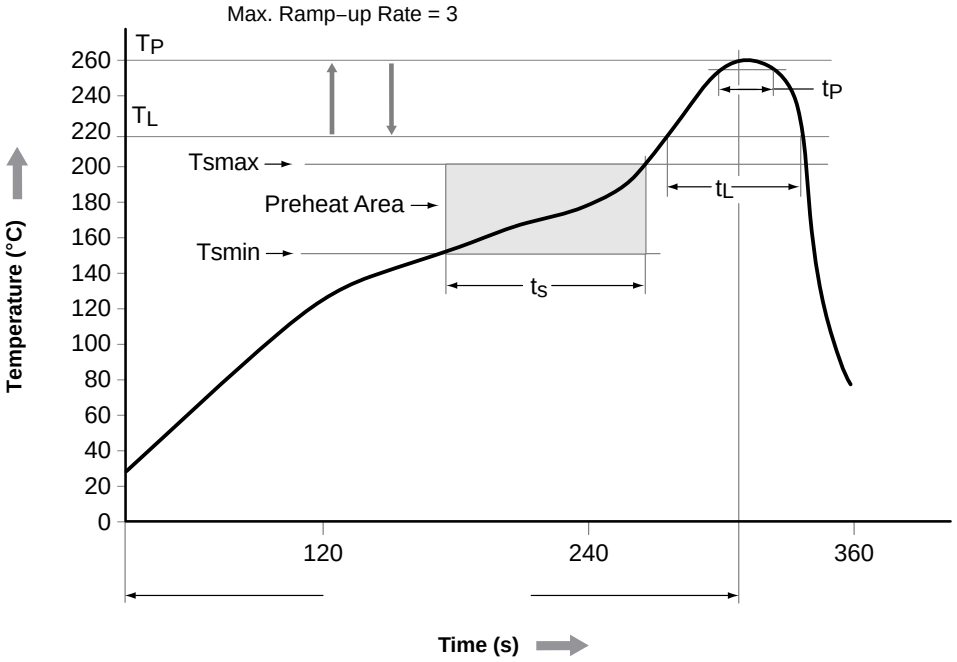


Figure 10. Switching Time Test Circuit

REFLOW PROFILE



ORDERING INFORMATION

Part Number (Note 7)	**Package**	**Packing Method**†
FOD050L	SOIC8 (Pb−Free)	Tube (50 Units per Tube)
FOD050LR2	SOIC8 (Pb−Free)	Tape and Reel (1000 Units per Reel)
FOD050LV	SOIC8 (Pb−Free), DIN EN/IEC60747−5−5 Option	Tube (50 Units per Tube)
FOD050LR2V	SOIC8 (Pb−Free), DIN EN/IEC60747−5−5 Option	Tape and Reel (1000 Units per Reel)

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

7. The product orderable part number system listed in this table also applies to the FOD053L product.

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