To learn more about ON Semiconductor, please visit our website at
www.onsemi.com

Block Diagram

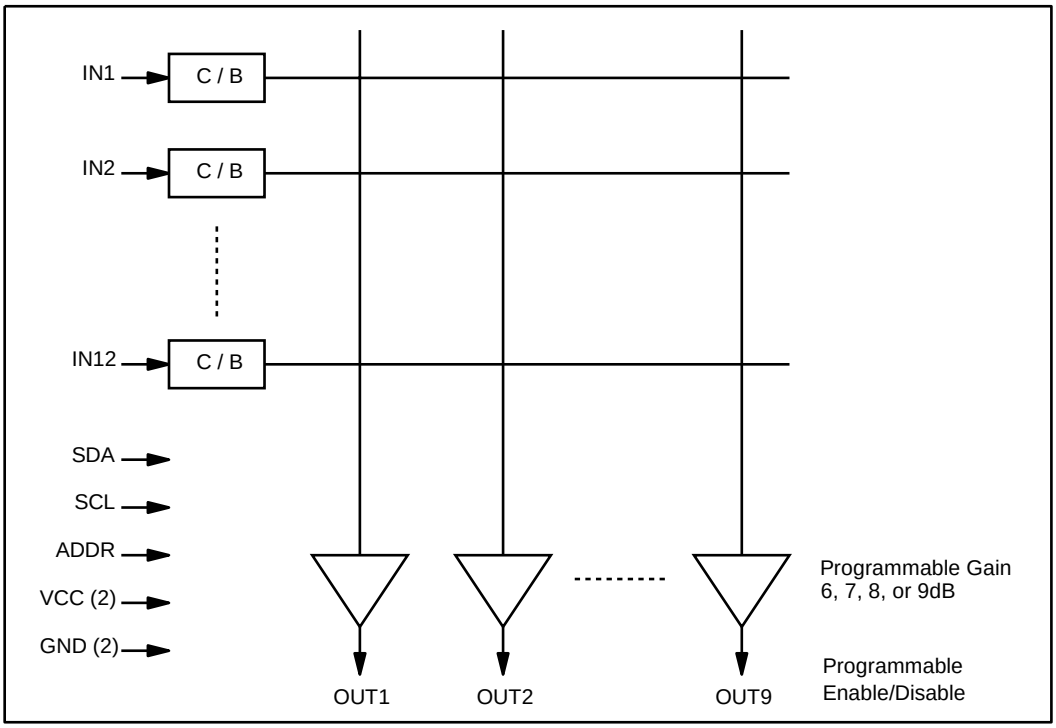


Figure 1. FMS6501 Block Diagram

Pin Configuration

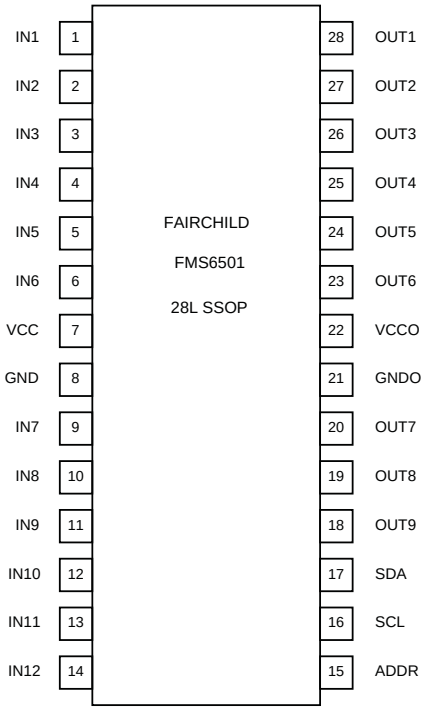


Figure 2. Pin Configuration

Pin Assignments

Pin#	Name	Type	Description
1	IN1	Input	Input, channel 1
2	IN2	Input	Input, channel 2
3	IN3	Input	Input, channel 3
4	IN4	Input	Input, channel 4
5	IN5	Input	Input, channel 5
6	IN6	Input	Input, channel 6
7	VCC	Input	Positive power supply
8	GND	Input	Must be tied to ground
9	IN7	Input	Input, channel 7
10	IN8	Input	Input, channel 8
11	IN9	Input	Input, channel 9
12	IN10	Input	Input, channel 10
13	IN11	Input	Input, channel 11
14	IN12	Input	Input, channel 12
15	ADDR	Input	Selects I^2C address. “0” = 0x06 (0000 0110), ‘1” = 0x86 (1000 0110)
16	SCL	Input	Serial clock for I^2C port
17	SDA	Input	Serial data for I^2C port
18	OUT9	Output	Output, channel 9
19	OUT8	Output	Output, channel 8
20	OUT7	Output	Output, channel 7
21	GNDO	Input	Must be tied to ground
22	VCCO	Input	Positive power supply for output drivers
23	OUT6	Output	Output, channel 6
24	OUT5	Output	Output, channel 5
25	OUT4	Output	Output, channel 4
26	OUT3	Output	Output, channel 3
27	OUT2	Output	Output, channel 2
28	OUT1	Output	Output, channel 1

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Parameter	Min.	Max.	Unit
DC Supply Voltage	-0.3	6.0	V
Analog and Digital I/O	-0.3	V_{cc} + 0.3	V
Output Current Any One Channel, Do Not Exceed		40	mA

Reliability Information

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_J	Junction Temperature			150	°C
T_{STG}	Storage Temperature Range	-65		150	°C
T_L	Lead Temperature (Soldering, 10 seconds)			300	°C
Θ					

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Electrostatic Discharge Protection

Digital Interface

The I^2C-compatible interface is used to program output enables, input to output routing, input clamp / bias, and output gain. The I^2C address of the FMS6501 is 0x06 (0000 0110) with the ability to offset it to 0x86 (1000 0110) by tying the ADDR pin high.

Both data and address data, of eight bits each, are written to the I^2C address to access all the control functions.

There are separate internal addresses for each output. Each output's address includes bits to select an input channel, adjust the output gain, and enable or disable the output amplifier. More than one output can select the same input channel for one-to-many routing. When the outputs are disabled, they are placed in a high-impedance state. This allows multiple FMS6501 devices to be paralleled to create a larger switch matrix. Typical output power-up time is less than 500ns.

The clamp / bias control bits are written to their own internal address, since they should always remain the same regardless of signal routing. They are set based on the input signal connected to the FMS6501.

All undefined addresses may be written without effect.

Output Control Register Contents and Defaults

Control Name	Width	Type	Default	Bit(s)	Description
Enable	1 bit	Write	0	7	Channel Enable: 1=Enable, 0=Power Down(1)
Gain	2 bits	Write	0	6:5	Channel Gain: 00=6dB, 01=7dB, 10=8dB, 11=9dB
Inx	5 bits	Write	0	4:0	Input selected to drive this output: 00000=OFF(2), 00001=IN1, 00010=IN2... 01100=IN12Clamp Contd8 -3w33[T Clamp Con

Notes:
1. Power down places the output in a high-impedance state so multiple FMS6501 devices may be paralleled. Power down also de-selects any input routed to the specified output.
2. When all inputs are OFF, the amplifier input is tied to approximately 150mV and the output goes to approximately 300mV with the 6dB gain setting.

Output Control Register MAP

Notes:
1. IN4 is provided for forward compatibility and should always be written as '0' in the FMS6501.

Clamp Control Register Contents and Defaults

Clamp Control Register Map

DC Electrical Characteristics

T_A = 25°C, V_{cc} = 5V, V_{IN} = 1V_{pp}, input bias mode, one-to-one routing, 6dB gain, all inputs AC coupled with 0.1µF, unused inputs AC-terminated through 75Ω to GND, all outputs AC coupled with 220µF into 150Ω loads, referenced to 400kHz, unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max	Units
I_{CC}	Supply Current[1]	No load, all outputs enabled		80	100	mA
V_{OUT}	Video Output Range			2.8		V_{pp}
R_{OFF}	Off Channel Output Impedance	Output disabled		3.0		kΩ
V_{clamp}	DC Output Level[1]	Clamp mode	0.2	0.3	0.4	V
V_{bias}	DC Output Level[1]	Bias mode	1.15	1.25	1.35	V
PSRR	Power Supply Rejection Ratio	All channels, DC		50		dB

Notes:
1. 100% tested at 25°C.

AC Electrical Characteristics

T_A = 25°C, V_{CC} = 5V, V_{IN} = 1V_{pp}, input bias mode, one-to-one routing, 6dB gain, all inputs AC coupled with 0.1µF, unused inputs AC-terminated through 75Ω to GND, all outputs AC coupled with 220µF into 150Ω loads, referenced to 400kHz, unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max	Units
AV_{SD}	Channel Gain(1) Error	All Channels, All Gain Settings, DC	-0.2	0	+0.2	dB
AV_{STEP}	Gain Step(1)	All Channels, DC	0.9	1.0	1.1	dB
f_{+1dB}	1dB Peaking Bandwidth	V_{OUT} = 1.4V_{pp}		65		MHz
f_{-1dB}	-1dB Bandwidth	V_{OUT} = 1.4V_{pp}		90		MHz
f_C	-3dB Bandwidth	V_{OUT} = 1.4V_{pp}		115		MHz
dG	Differential Gain	3.58MHz		0.1		%
dP	Differential Phase	3.58MHz		0.2		deg
THD_{SD}	SD Output Distortion	V_{OUT} = 1.4V_{pp}, 5MHz		0.05		%
THD_{HD}	HD Output Distortion	V_{OUT} = 1.4V_{pp}, 22MHz		0.6		%
X_{TALK1}	Input Crosstalk	1MHz, V_{OUT} = 2V_{pp}(2)		-72		dB
X_{TALK2}						

Notes:
1. 100% tested at 25°C.
2. Adjacent input pair to adjacent output pair. Interfering input is through an open switch.
3. Adjacent input pair to adjacent output pair. Interfering input is through a closed switch.
4. Crosstalk of eight synchronous switching outputs onto single, asynchronous switching output.
5. Signal-to-Noise Ration (SNR) = 20 * log (714mV / rms noise).

FMS6501 — 12 Input / 9 Output Video Switch Matrix with Input Clamp, Input Bias Circuitry, and Output Drivers

Acknowledge

The data bytes transferred between the START and STOP conditions from transmitter to receiver is unlimited. Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a high-level signal put on the bus by the transmitter, during which the master generates an extra acknowledge-related clock pulse. A slave receiver must generate an acknowledge after the reception of each byte. A master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges must pull down the SDA line during the acknowledge clock pulse so the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

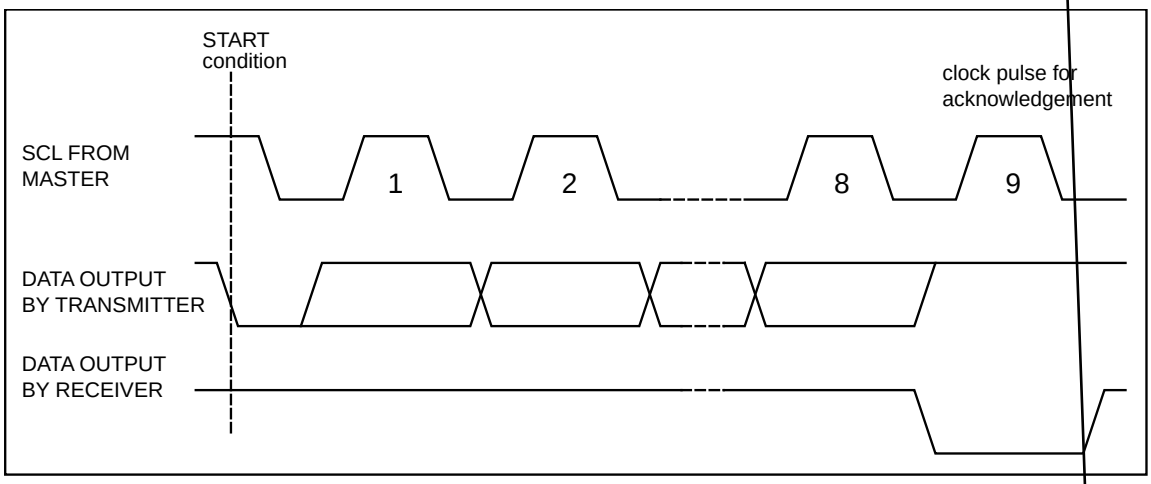


Figure 6. Acknowledgement on the I²C Bus

I²C Bus Protocol

Before any data is transmitted on the I²C bus, the device that should respond is addressed first. The addressing is always carried out with the first byte transmitted after the start procedure. The I²C bus configuration for a data write to the FMS6501 is shown in Figure 5.

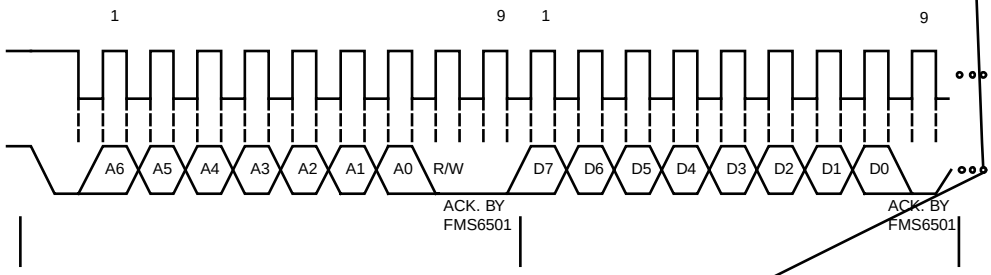


Figure 7. Write a Register Address to the Pointer Register, Then Write Data to the Selected Register

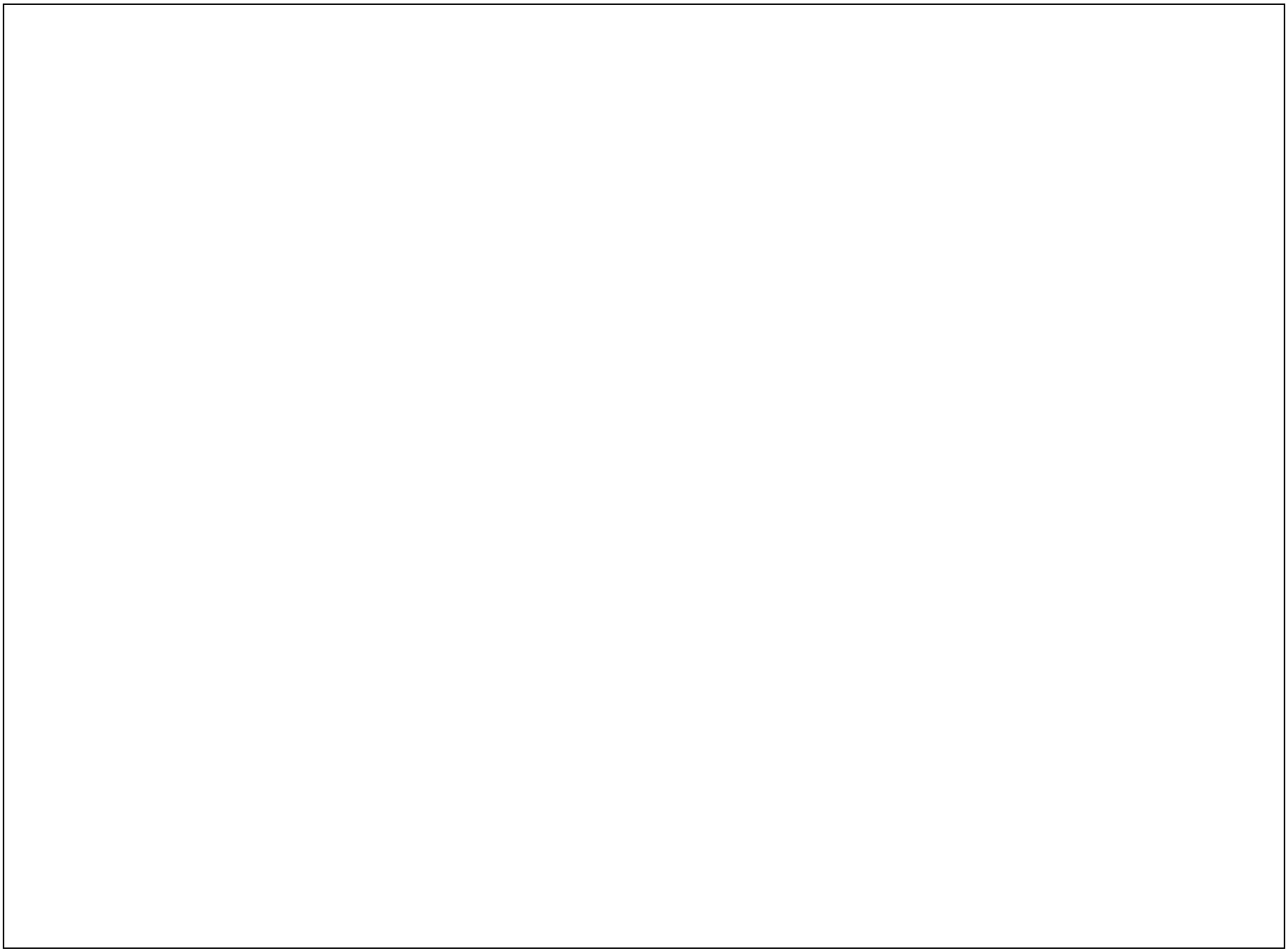
Applications Information

Input Clamp / Bias Circuitry

The FMS6501 accommodates AC- or DC-coupled inputs.

Internal clamping and bias circuitry are provided to sup-

FMS6501 — 12 Input / 9 Output Video Switch Matrix with Input Clamp, Input Bias Circuitry, and Output Drivers



Layout Considerations

General layout and supply bypassing play major roles in high-frequency performance and thermal characteristics. Fairchild offers a demonstration board, FMS6501DEMO, to use as a guide for layout and to aid in device testing and characterization. The FMS6501DEMO is a 4-layer board with a full power and ground plane. For optimum results, follow the steps below as a basis for high frequency layout.

- Include 10µF and 0.1µF bypass capacitors.
- Place the 10µF capacitor within 0.75 inches of the power pin.
- Place the 0.1µF capacitor within 0.1 inches of the power pin.
- Connect all external ground pins as tightly as possible, preferably with a large ground plane under the package.
- Layout channel connections to reduce mutual trace inductance.
- Minimize all trace lengths to reduce series inductances. If routing across a board, place device such that longer traces are at

Physical Dimensions

Dimensions are in millimeters unless otherwise noted.

SSOP-28

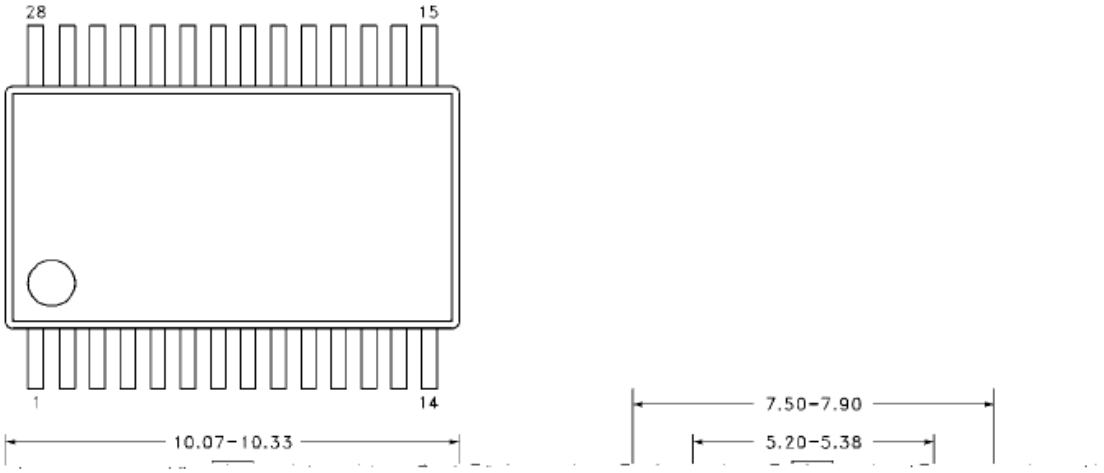


Figure 15. FMS6501 28-Lead Small Scale Outline Package (SSOP)

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5817−1050

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative