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FMS6363A — Three-Channel 7th-Order High-Definition VoltagePlus™ Video Filter Driver

Block Diagram

IN1

IN2

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

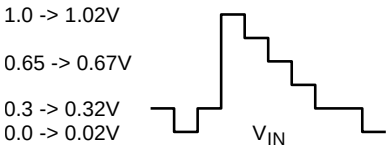
Symbol	Parameter	Min.	Max.	Unit
V_S	DC Supply Voltage	-0.3	6.0	V
V_{IO}	Analog and Digital I/O	-0.3	V_{CC}+0.3	V
V_{OUT}				

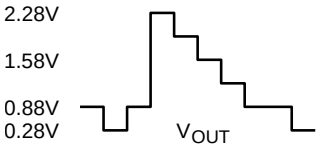
Typical Application

Application Information

Application Circuits

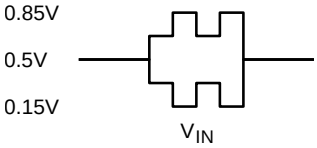
The FMS6363A VoltagePlus™ video filter provides 6dB gain from input to output. In addition, the input is slightly offset to optimize the output driver performance. The offset is held to the minimum required value to decrease the standing DC current into the load. Typical voltage levels are shown in Figure 4:

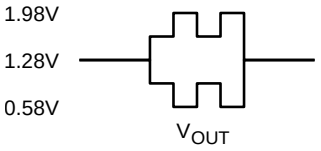




Driven by:
DC-Coupled DAC Outputs
AC-Coupled and Clamped
Y, CV, R, G, B

There is a 280mV offset from the DC input level to the DC output level. $V_{OUT} = 2 * V_{IN} + 280mV$.





Driven by:
AC-Coupled and Biased
U, V, Pb, Pr, C

The same method can be used for biased signals. The Pb and Pr channels are baised to set the DC level to 500mV.

Figure 9. Biased SCART with DC-Coupled Outputs

The same circuits can be used with AC-coupled outputs if desired.

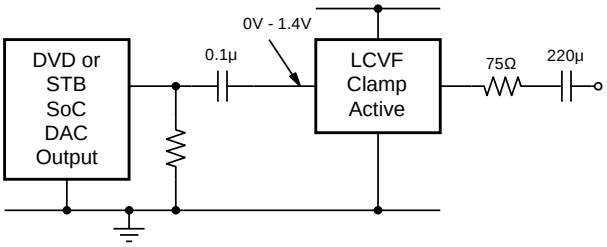
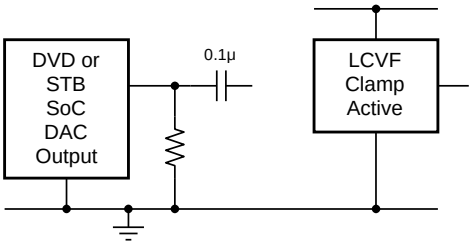


Figure 10. DC-Coupled Inputs, AC-Coupled Outputs



Layout Considerations

General layout and supply bypassing play a major role in high-frequency performance and thermal characteristics. Fairchild offers a evaluation board to guide layout and aid device evaluation. The evaluation board is a four-layer board with full power and ground planes. Following this layout configuration provides optimum performance and thermal characteristics for the device. For the best results, follow the steps and recommended routing rules listed below.

Recommended Routing / Layout Rules

Do not run analog and digital signals in parallel.

Use separate analog and digital power planes to supply power.

Traces should run on top of the ground plane at all times.

No trace should run over ground/power splits.

Avoid routing at 90° angles.

Minimize clock and video data trace length differences.

Include 10µF and 0.1µF ceramic power supply bypass capacitors.

Place the 0.1µF capacitor within 2.54mm (0.1in) of the device power pin.

Place the 10µF capacitor within 19.05mm (0.75in) of the device power pin.

For multi-layer boards, use a large ground plane to help dissipate heat.

For two-layer boards, use a ground plane that extends beyond the device body at least 12.7mm (0.5in) on all sides. Include a metal paddle under the device on the top layer.

Minimize all trace lengths to reduce series inductance.

Output Considerations

The FMS6363A outputs are DC offset from the input by 150mV; therefore, $V_{OUT} = 2 \bullet V_{IN}$ DC+150mV. This offset is required to obtain optimal performance from the output driver and is held at the minimum value to decrease the standing DC current into the load. Since the FMS6363A has a 2x (6dB) gain, the output is typically connected via a 75Ω-series back-matching resistor followed by the 75Ω video cable. Due to the inherent divide-by-two of this configuration, the blanking level at the load of the video signal is always less than 1V. When AC-coupling the output, ensure that the coupling capacitor of choice passes the lowest frequency content in the video signal and that line time distortion (video tilt) is kept as low as possible.

The selection of the coupling capacitor is a function of the subsequent circuit i