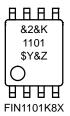


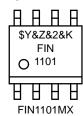




US8 CASE 846AN

MARKING DIAGRAM





\$Y = Logo

&Z = Assembly Plant Code &2 = 2-Digit Date Code

&K = 2-Digits Lot Run Traceability Code

1101, FIN1101 = Specific Device Code

CONNECTION DIAGRAMS

_	
 -	_
	_

SOIC Package

•	
R _{IN} _	Inverting LVDS Inputs
D _{OUT+}	Non-Inverting Driver Outputs
D _{OUT}	Inverting Driver Outputs
EN	Driver Enable Pin
V _{CC}	Power Supply
GND	Ground

FUNCTION TABLE

Inputs			Outputs		
EN	R _{IN+}	R _{IN} _	D _{OUT+} D _{OUT}		
Н	Н	L	Н	L	
Н	L	Н	L	Н	
Н	Fail Safe Case		Н	L	
L	Х	Х	Z	Z	

H = HIGH Logic Level X = Don't Care L = LOW Logic Level Z = High Impedance

ORDERING INFORMATION

See detailed ordering and shipping information on page 4 of this data sheet.

FIN1101

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rating
V _{CC}	Supply Voltage	-0.5 V to +4.6 V
V_{IN}	LVDS DC Input Voltage	–0.5 V to +4.6 V

 V_{OUT}

FIN1101

AC ELECTRICAL CHARACTERISTICS (Over supply voltage and operating temperature ranges, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ (Note 2)	Max	Unit	
t _{PLHD}	Differential Propagation Delay LOW-to-HIGH	$R_L = 100 \Omega$, $C_L = 5 pF$,	0.75	1.1	1.75	ns	
t _{PHLD}	Differential Propagation Delay HIGH-to-LOW	$V_{ID} = 200 \text{ mV to } 450 \text{ mV,}$ $V_{IC} = V_{ID} / 2 \text{ to } (V_{CC} - (V_{ID} / 2),)$	0.75	1.1	1.75	ns	
t _{TLHD}	Differential Output Rise Time (20% to 80%)	Duty Cycle = 50%, See Figure 3 and Figure 4	0.29	0.40	0.58	ns	
t _{THLD}	Differential Output Fall Time (80% to 20%)		0.29	0.40	0.58	ns	
t _{SK(P)}	Pulse Skew t _{PLH} - t _{PHL}		_	0.01	0.2	ns	
t _{SK(PP)}	Part-to-Part Skew (Note 3)		_	_	0.5	ns	
f_{MAX}	Maximum Frequency (Note 4) (Note 5)		400	800	-	MHz	
t _{PZHD}	Differential Output Enable Time from Z to HIGH	$R_L = 100 \Omega$, $C_L = 5 pF$, See Figure 2	_	2.1	5	ns	
t _{PZLD}	Differential Output Enable Time from Z to LOW	and Figure 3	_	2.3	5	ns	
t _{PHZD}	•			-		-	-

FIN1101

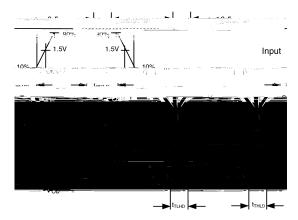
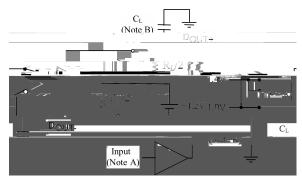


Figure 4. AC Waveforms



Note A: All LVTTL input pulses have frequency = 10 MHz, t_R or $t_F \le 2$ ns Note B: C_L includes all probe and test fixture capacitances

Figure 5. Differential Driver Enable and Disable Test Circuit

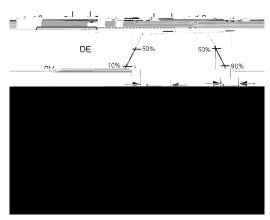


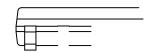
Figure 6. Enable and Disable AC Waveforms

ORDERING INFORMATION

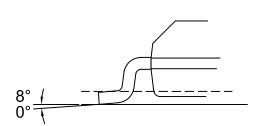
Order Number	Package Number	Package Description	Shipping [†]
FIN1101MX			

DATE 24 AUG 2017

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