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Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain

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FIN1031
3.3V LVDS 4-Bit High Speed Differential Driver

General Description

This quad driver is designed for high speed interconnects utilizing Low Voltage Differential Signaling (LVDS) technology. The driver translates LVTTL signal levels to LVDS levels with a typical differential output swing of 350mV which provides low EMI at ultra low power dissipation even at high frequencies. This device is ideal for high speed transfer of clock and data.

The FIN1031 can be paired with its companion receiver, the FIN1032, or any other Fairchild LVDS receiver.

Features

- Greater than 400Mbs data rate
- 3.3V power supply operation
- 0.4ns maximum differential pulse skew
- 2.0ns maximum propagation delay
- Low power dissipation
- Power OFF protection
- Meets or exceeds the TIA/EIA-644 LVDS standard
- Pin compatible with equivalent RS-422 and LVPECL devices
- 16-Lead SOIC and TSSOP packages save space

Ordering Code:

Order Number	Package Number	Package Description
FIN1031M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
FIN1031MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

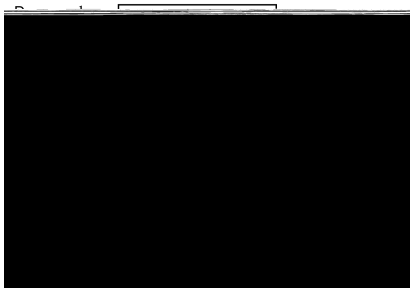
Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Function Table

Inputs			Outputs	
EN	$\overline{EN}$	D_{IN}	D_{OUT+}	D_{OUT-}
H	X	H	H	L
H	X	L	L	H
H	X	OPEN	L	H
X	L	H	H	L
X	L	L	L	H
X	L	OPEN	L	H
L	H	X	Z	Z

H = HIGH Logic Level L = LOW Logic Level
X = Don't Care Z = High Impedance

Connection Diagram



Pin Descriptions

Pin Name	Description
D_{IN1}, D_{IN2}, D_{IN3}, D_{IN4}	LVTTL Data Inputs
D_{OUT1+}, D_{OUT2+}, D_{OUT3+}, D_{OUT4+}	Non-Inverting Driver Outputs
D_{OUT1-}, D_{OUT2-}, D_{OUT3-}, D_{OUT4-}	Inverting Driver Outputs
EN	Driver Enable Pin
$\overline{EN}$	Inverting Driver Enable Pin
V_{CC}	Power Supply
GND	Ground

Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC})	−0.5V to +4.6V

Recommended Operating Conditions

Note 1: The "Absolute Maximum Ratings": are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature and output/input loading variables. Fairchild does not recommend operation of circuits outside databook specification.

DC Electrical Characteristics

Over supply voltage and operating temperature ranges, unless otherwise specified

Note 2: All typical values are at $T_A = 25°C$ and with $V_{CC} = 3.3V$.

AC Electrical Characteristics

Over supply voltage and operating temperature ranges, unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ (Note 3)	Max	Units
t_{PLHD}	Differential Propagation Delay LOW-to-HIGH	R_L = 100 Ω, C_L = 10 pF, See Figure 2 and Figure 3 (Note 7)	0.8	1.4	2.0	ns
t_{PHLD}	Differential Propagation Delay HIGH-to-LOW		0.8	1.4	2.0	ns
t_{TLHD}	Differential Output Rise Time (20% to 80%)		0.6	0.85	1.2	ns
t_{THLD}	Differential Output Fall Time (80% to 20%)		0.6	0.85	1.2	ns
$t_{SK(P)}$	Pulse Skew $\lvert t_{PLH} - t_{PHL} \rvert$				0.4	ns
$t_{SK(LH)}$ $t_{SK(HL)}$	Channel-to-Channel Skew (Note 4)				0.3	ns
$t_{SK(PP)}$	Part-to-Part Skew (Note 5)				1.0	ns
f_{MAX}	Maximum Frequency (Note 6)		200	275		MHz
t_{ZHD}	Differential Output Enable Time from Z to HIGH	R_L = 100Ω, C_L = 10 pF, See Figure 4 and Figure 5 (Note 7)		2.5	5.0	ns
t_{ZLD}	Differential Output Enable Time from Z to LOW			2.7	5.0	ns
t_{HZD}	Differential Output Disable Time from HIGH to Z			3.2	5.0	ns
t_{LZD}	Differential Output Disable Time from LOW to Z			3.4	5.0	ns

Note 3: All typical values are at T_A = 25°C and with V_{CC} = 3.3V.

Note 4: $t_{SK(LH)}$, $t_{SK(HL)}$ is the skew between specified outputs of a single device when the outputs have identical loads and are switching in the same direction.

Note 5: $t_{SK(PP)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices switching in the same direction (either LOW-to-HIGH or HIGH-to-LOW) when both devices operate with the same supply voltage, same temperature, and have identical test circuits.

Note 6: f_{MAX} Criteria: Input $t_R = t_F$ < 1 ns, 0V to 3V, 50% Duty Cycle; Output V_{OD} > 250 mV, 45% to 55% Duty Cycle; all output channels switching in phase.

Note 7: Test Circuits in Figure 2 and Figure 4 are simplified representations of test fixture and DUT loading.

FIGURE 1. Differential Driver DC Test Circuit

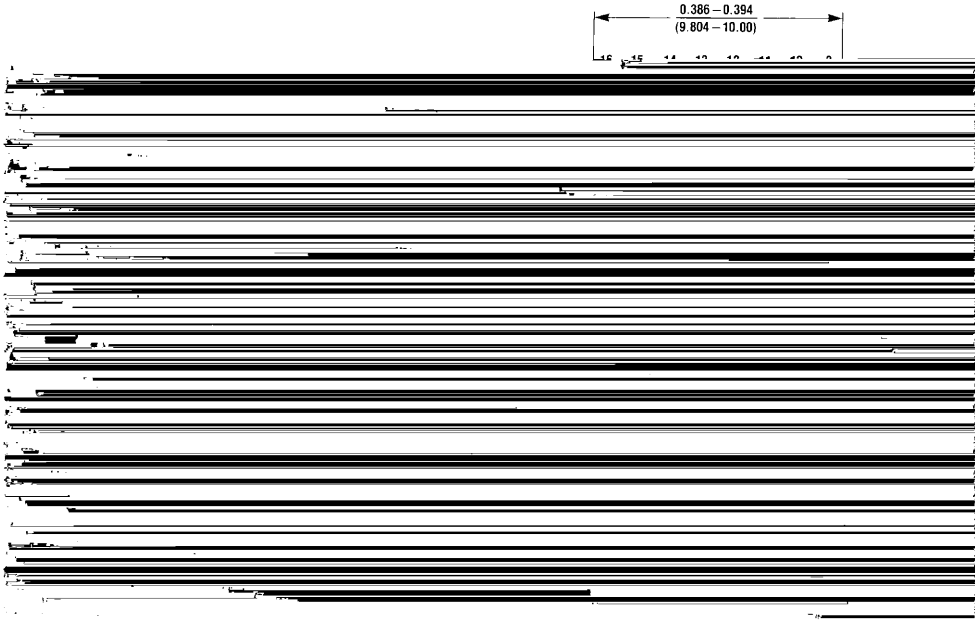
Note A: All input pulses have frequency = 10 MHz, t_R or t_F = 1 ns
Note B: C_L includes all fixture and instrumentation capacitances

FIGURE 2. Differential Driver Propagation Delay and Transition Time Test Circuit

Note B: All input pulses have the frequency =

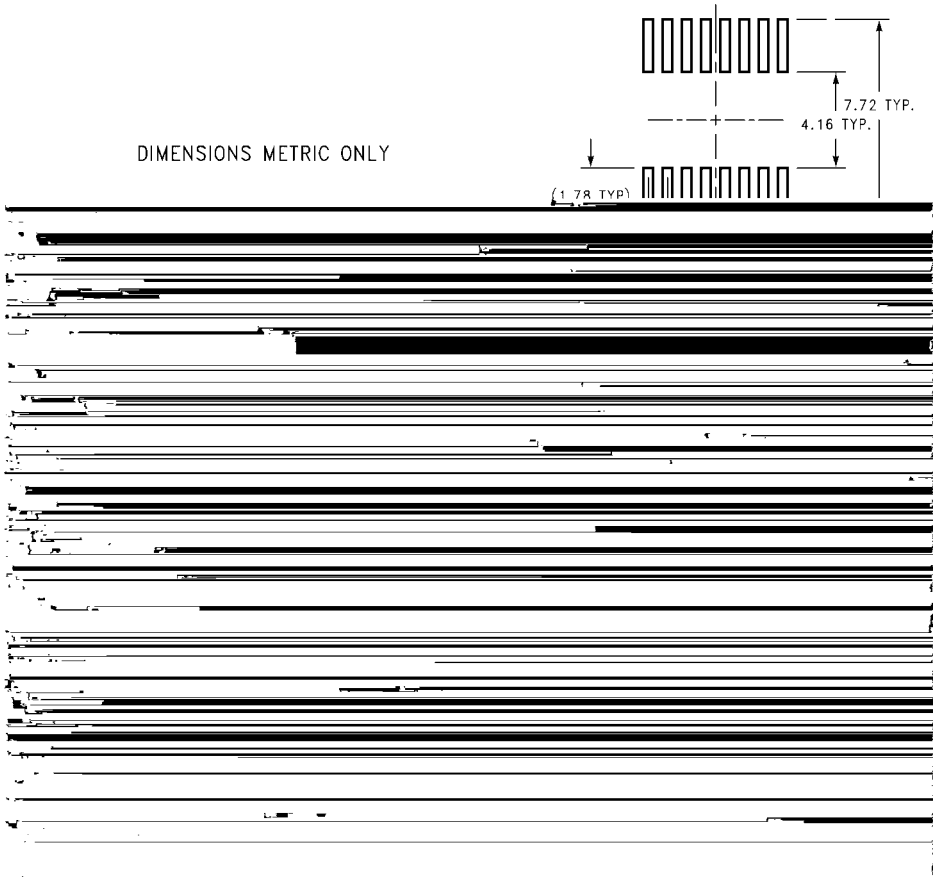
FIGURE 3. AC Waveforms

Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M16A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC16

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