## Is Now Part of

## To learn more about ON Semiconductor, please visit our website at
## www.onsemi.com

Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

---

September 2001
Revised December 2001

# FIN1022
# 2 X 2 LVDS High Speed Crosspoint Switch

## General Description

This non-blocking 2x2 crosspoint switch has a fully differential input to output data path for low noise generation and low pulse width distortion. The device can be used as a

 

## AC Electrical Characteristics

Over supply voltage and operating temperature ranges, unless otherwise specified

| Symbol | Parameter | Test Conditions | Min | Typ (Note 4) | Max | Units |
|---|---|---|---|---|---|---|
| $t_{PLHD}$ | Differential Output Propagation Delay | | 0.7 | | 1.6 | ns |
| | LOW-to-HIGH | $R_L$ = 75 Ω, $C_L$ = 5 pF, | 1.0 | 1.2 | 1.3 | |
| $t_{PHLD}$ | Differential Output Propagation Delay | $V_{CC}$ = 3.3V, $T_A$ = 25°C | 0.7 | | 1.6 | ns |
| | HIGH-to-LOW | See Figure 4 and Figure 5 | 1.0 | 1.2 | 1.3 | |
| $t_{TLHD}$ | Differential Output Rise Time (20% to 80%) | | 290 | | 580 | ps |
| $t_{THLD}$ | Differential Output Fall Time (80% to 20%) | | 290 | | 580 | ps |
| $t_{PLH}$ | Selection Propagation Delay | | 0.6 | | 1.5 | ns |
| | LOW-to-HIGH ($SEL_n$ to $OUT_n$) | $R_L$ = 75 Ω, $C_L$ = 5 pF, | 0.9 | 1.1 | 1.2 | |
| $t_{PHL}$ | Selection Propagation Delay | $V_{CC}$ = 3.3V, $T_A$ = 25°C | 0.6 | | 1.5 | ns |
| | HIGH-to-LOW ($SEL_n$ to $OUT_n$) | See Figure 6 and Figure 7 | 0.9 | 1.1 | 1.2 | |
| $t_{ZHD}$ | | | | | | |

**Note 4:** All typical values are at $T_A$ = 25°C and with $V_{CC}$ = 3.3V.

**Note 5:** Part-to-part skew is the maximum delay time difference on like edges (LOW-to-HIGH or HIGH-to-LOW) for the same $V_{CC}$ and temperature conditions.

## Required Specifications

1. When the true and complement LVDS outputs (having a 75Ω connected between outputs) are connected to 3.75 kΩ resistors and the common point of those 3.75 kΩ resistors are connected to a voltage source that sweeps from 0 to 2.4V, the DC $V_{OD}$ and $\Delta V_{OD}$ are still maintained (see Figure 1).
2. When the true and complement LVDS outputs (having a 5 pF capacitor attached between outputs) are connected with 37.5Ω resistors each to common point, then the common point does not vary by more than 150 mV under all process, temperature and voltage conditions when the outputs switch either from LOW-to-HIGH or from HIGH-to-LOW (see Figure 2).

## Required Specifications (Continued)

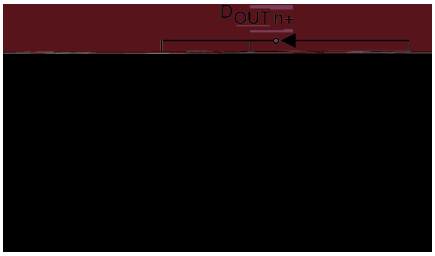


**FIGURE 3. LVDS Driver DC Test Circuit**

Note A: All input pulses have frequency = 50 MHz, $t_R$ or $t_F$ = 500 ps
Note B: $C_L$ includes all probe and jig capacitances

**FIGURE 4. LVDS Input to LVDS Driver Propagation Delay and Transition Time Circuit**

**FIGURE 5. LVDS Input to LVDS Output AC Waveforms**

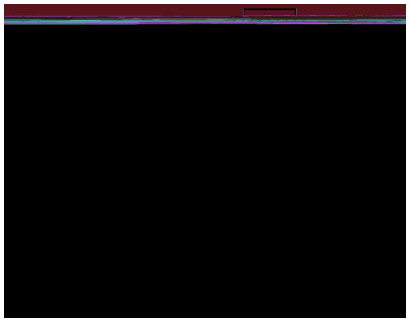

**FIGURE 6. LVTTL Input to LVDS Driver Propagation Delay and Transition Time Test Circuit**

## Required Specifications (Continued)

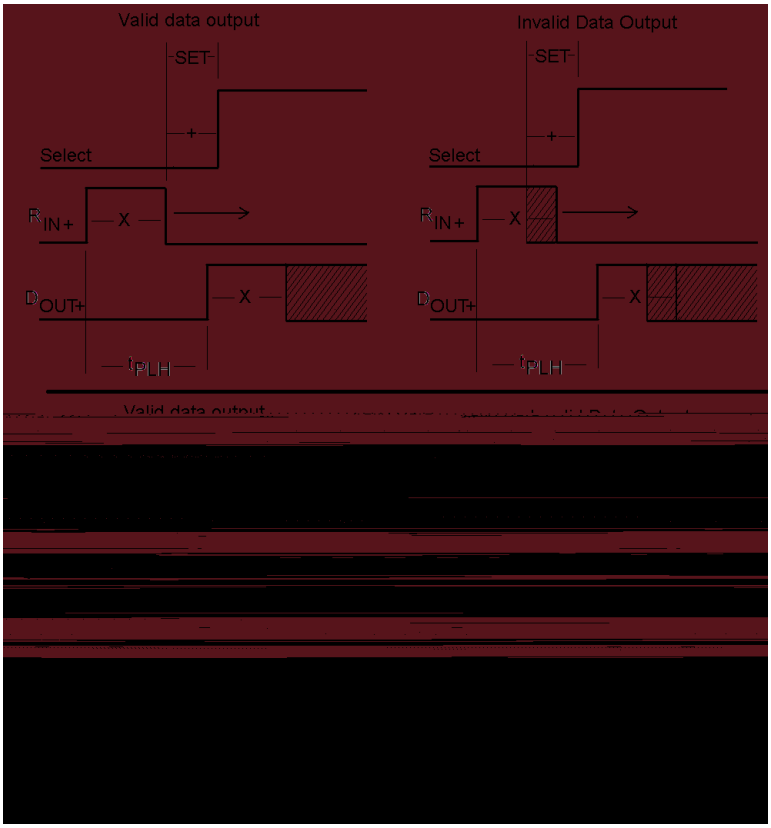


**FIGURE 10. Set-up and Hold Time Specification**

## PUBLICATION ORDERING INFORMATION

**N. American Technical Support**: 800−282−9855 Toll Free
USA/Canada
**Europe, Middle East and Africa Technical Support:**