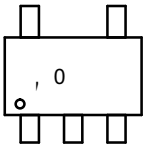
LVDS 1-B , H -S
D I a R I v

FIN1002

Description

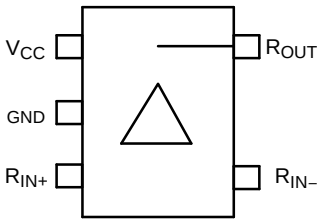
This single receiver is designed for high−speed interconnects utilizing Low Voltage Differential Signaling (LVDS) technology. The receiver translates LVDS levels, with a typical differential input threshold of 100 mV, to LVTTL signal levels. LVDS provides low EMI at ultra low power dissipation even at high frequencies. This device is ideal for high−speed transfer of clock or data. The FIN1002 can be paired with its companion driver, the FIN1001, or with any other LVDS driver.



Features

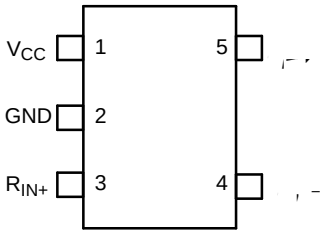
- Greater than 400 Mbs Data Rate
- 3.3 V Power Supply Operation
- 0.4 ns Maximum Pulse Skew
- 2.5 ns Maximum Propagation Delay
- Bus Pin ESD (HBM) Protection Exceeds 10 kV
- Power−Off, Over−voltage Tolerant Input and Output
- Fail−safe Protection for open−circuit and Non−driven, Shorted, or Terminated Conditions
- High−impedance Output at V_{CC} < 1.5 V
- Meets or exceeds TIA/EIA−644 LVDS Standard
- 5−Lead SOT23 Package Saves Space

CONNECTION DIAGRAM



(Top View)

PIN CONFIGURATION



PIN DEFINITIONS

Pin No.	Function	Description
1	V_{CC}	Power Supply
2	GND	Ground for the IC
3	R_{IN+}	Non−inverting Driver Input
4	$R_{IN−}$	Inverting Driver Input
5	R_{OUT}	LVTTL Data Output

FUNCTION TABLE

Inputs		Outputs
, +	, -	

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	–0.	4.6	V
R_{IN+} / R_{IN-}	Input Voltage	–0.	4.6	V
D_{OUT}	DC Output Voltage	–0.	6.0	V
I_O	Output Current		16	mA
T_{STG}	Storage Temperature Range	65	+150	°C
T_J	Maximum Junction Temperature		+150	

AC ELECTRICAL CHARACTERISTICS

All min. and max. values are guaranteed at T_A = −40 to +85°C. All typical values are at T_A = 25°C and with V_{CC} = 3.3 V, unless otherwise specified.
$|V_{ID}|$ = 400 mV, C_L = 10 pF. See Figure 1 and Figure 2.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_{PLH}	Propagation Delay	LOW to HIGH	0.9	1.5	2.5	ns
t_{PHL}	Propagation Delay	HIGH to LOW	0.9	1.5	2.5	ns
t_{TLH}	Output Rise Time	20% to 80%		0.6		ns
t_{THL}	Output Fall Time	80% to 20%		0.5		ns
$t_{SK(p)}$	Pulse Skew	$\|t_{PLH} - t_{PHL}\|$		0.02	0.4	ns
$t_{SK(PP)}$	Part−to−Part Skew (Note 2)				1.0	ns

2. $t_{SK(PP)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices switching in the same direction same

TYPICAL CHARACTERISTICS

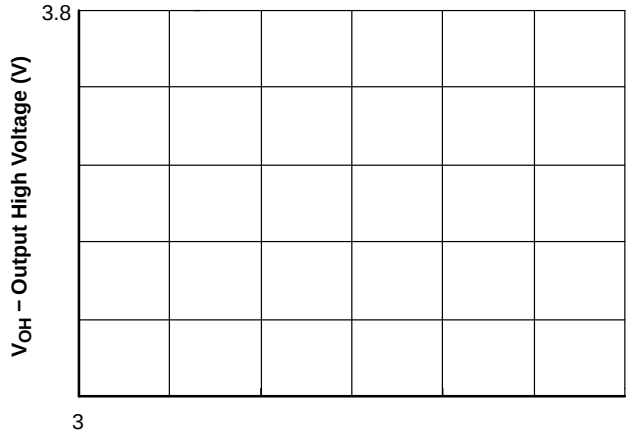


Figure 3. Output High Voltage vs. Power Supply Voltage

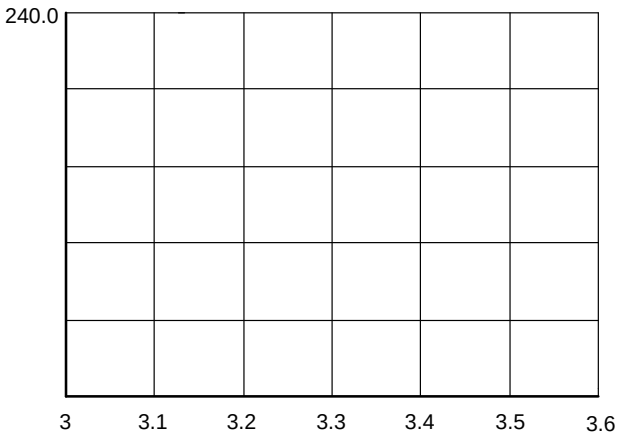


Figure 4. Output Low Voltage vs. Power Supply Voltage

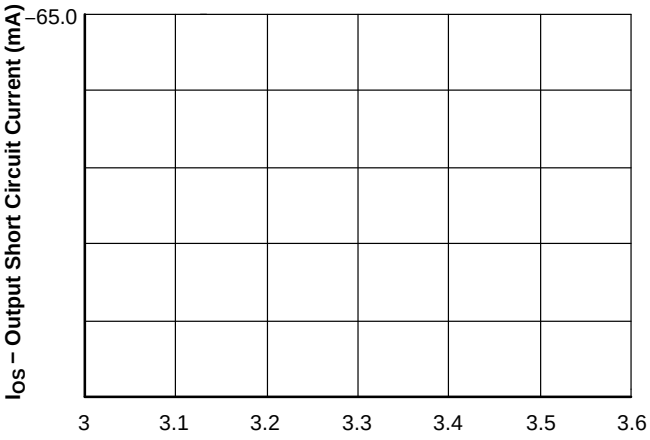


Figure 5. Output Short Circuit Current vs. Power Supply Voltage

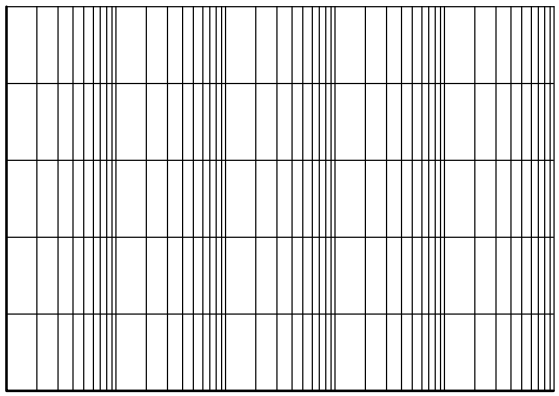
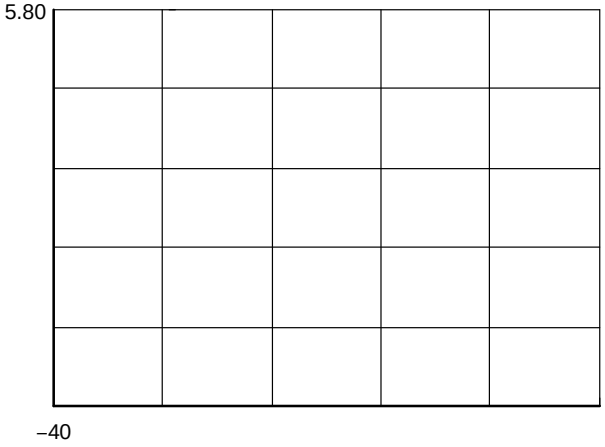
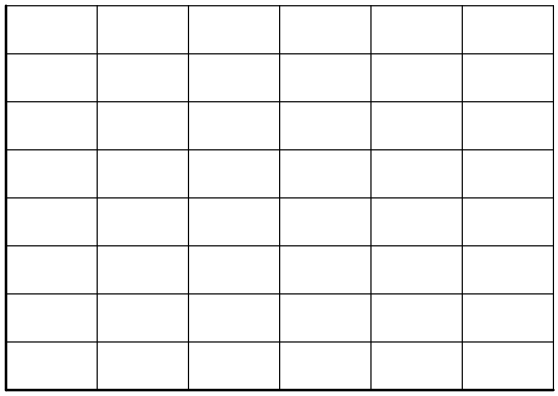
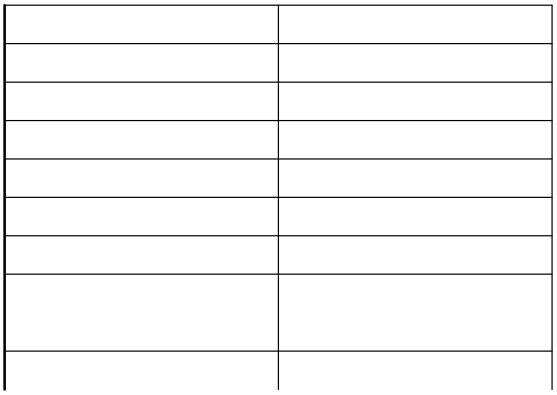


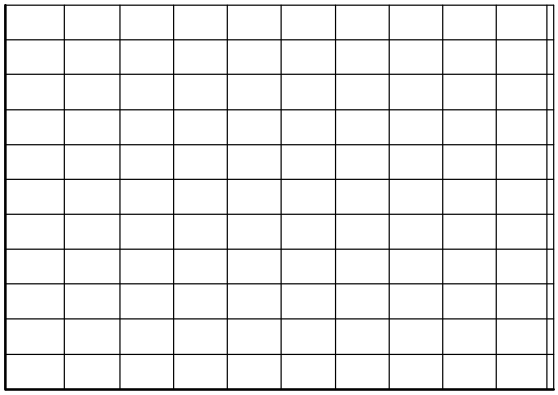
Figure 6. Power Supply Current vs. FrequencyOS

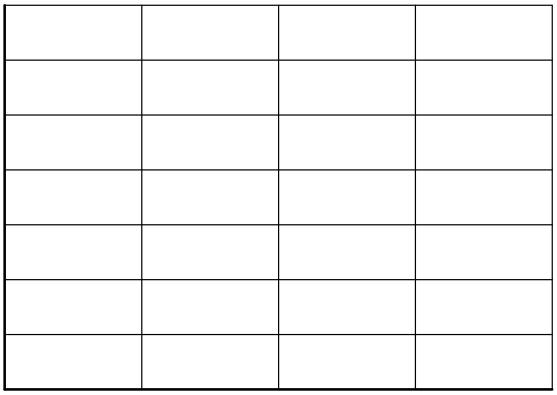


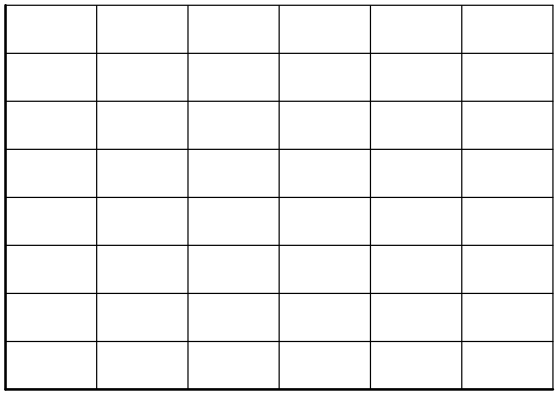


TYPICAL CHARACTERISTICS (continued)





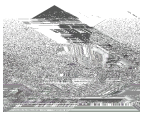




ORDERING INFORMATION

Product Number	Package	Shipping†
FIN1002M5X	5 Lead SOT23, JEDEC MO−178, 1.6 mm (Pb−Free)	3000 / Tape and Reel

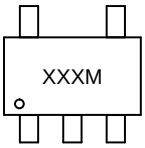
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



SOT 23, 5 Lead
CASE 527AH
ISSUE A

DATE 09 JUN 2021

GENERIC
MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code

*This information is generic. Please refer to