

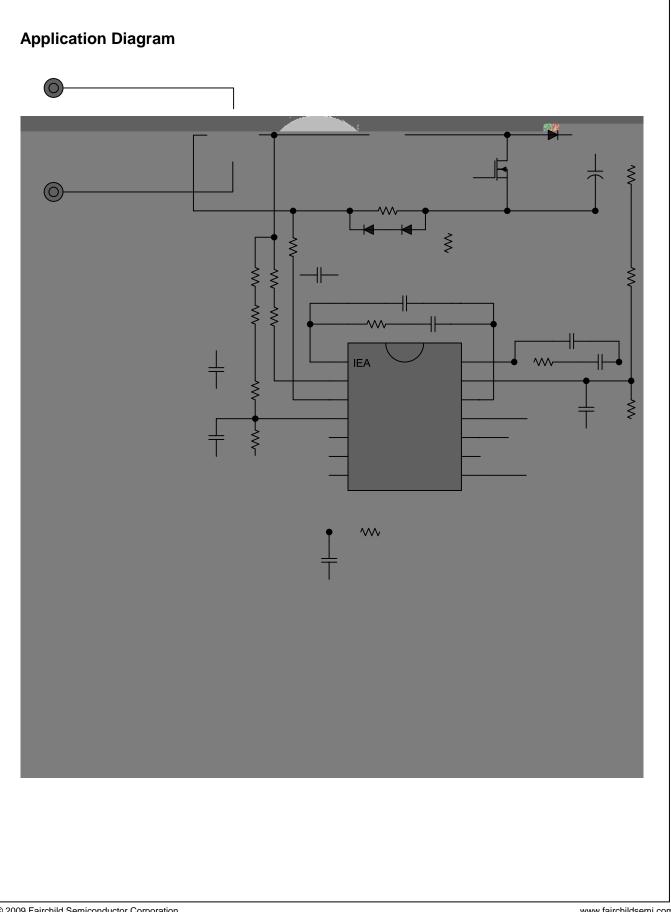
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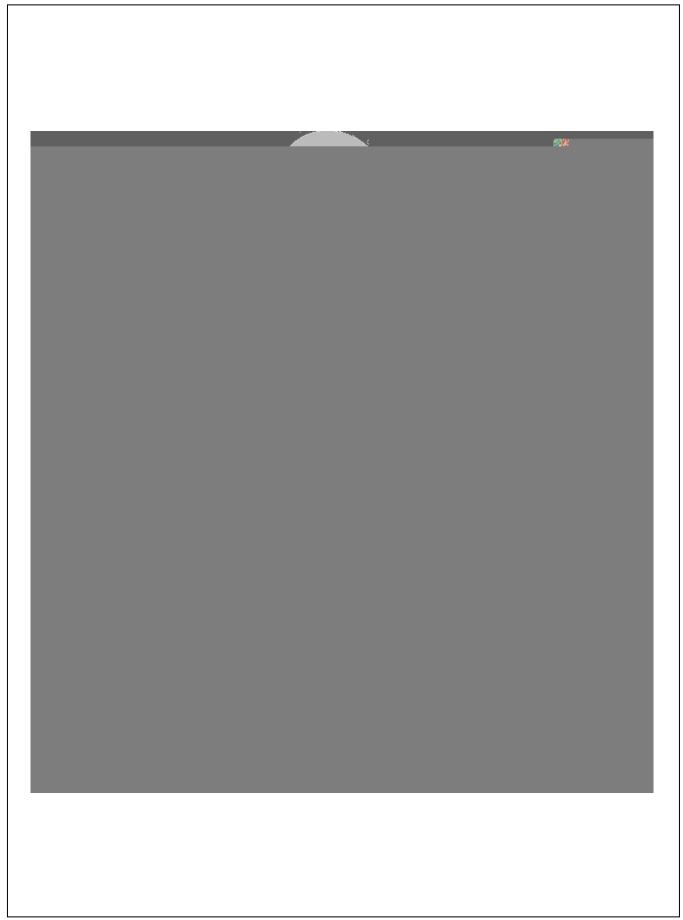
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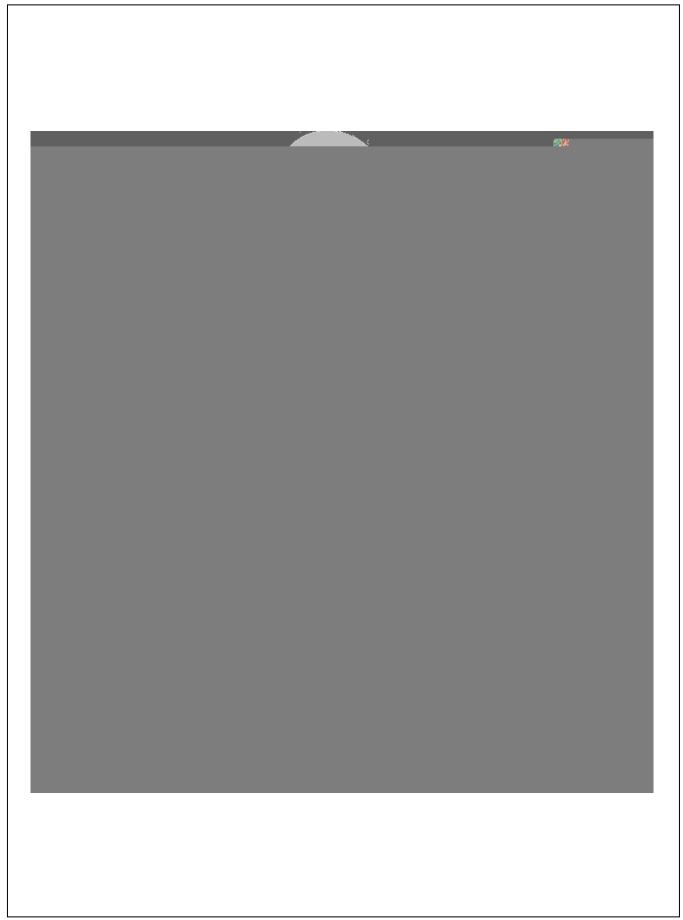




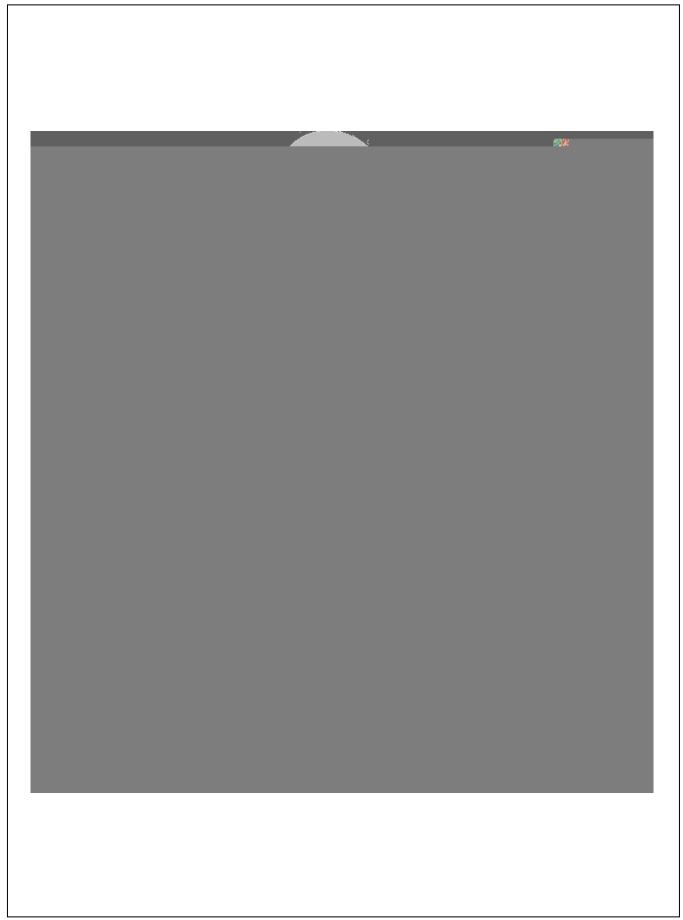


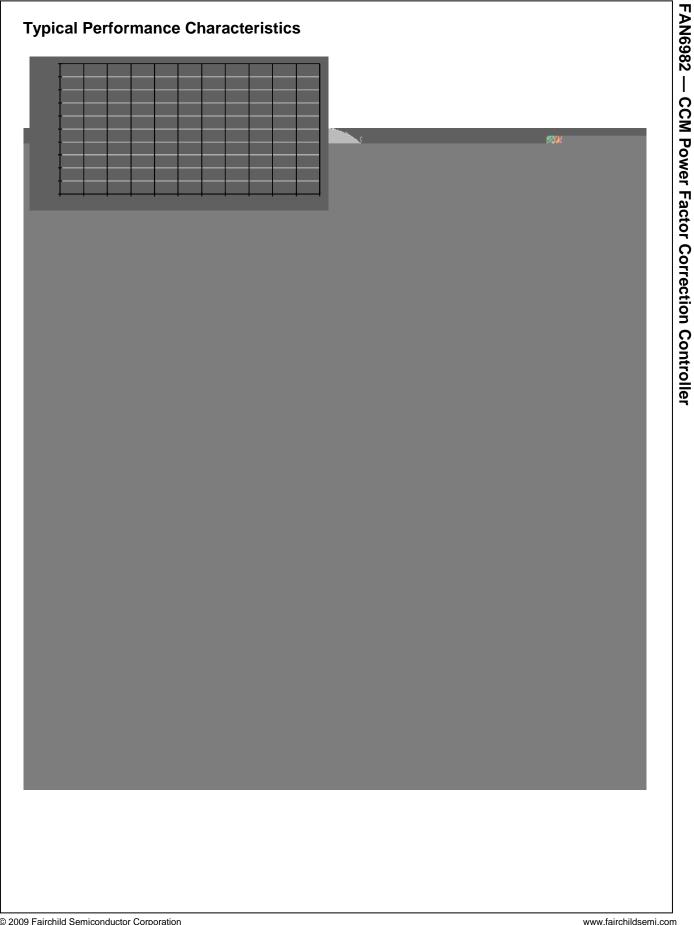
Pin Configuration			
	IEA		
	IAC		<i>™R</i>
	ISENSE	VREF	
	VRMS	VDD	
	RDY	OPFC	
	EN	PGND	
	RT/CT	SGND	



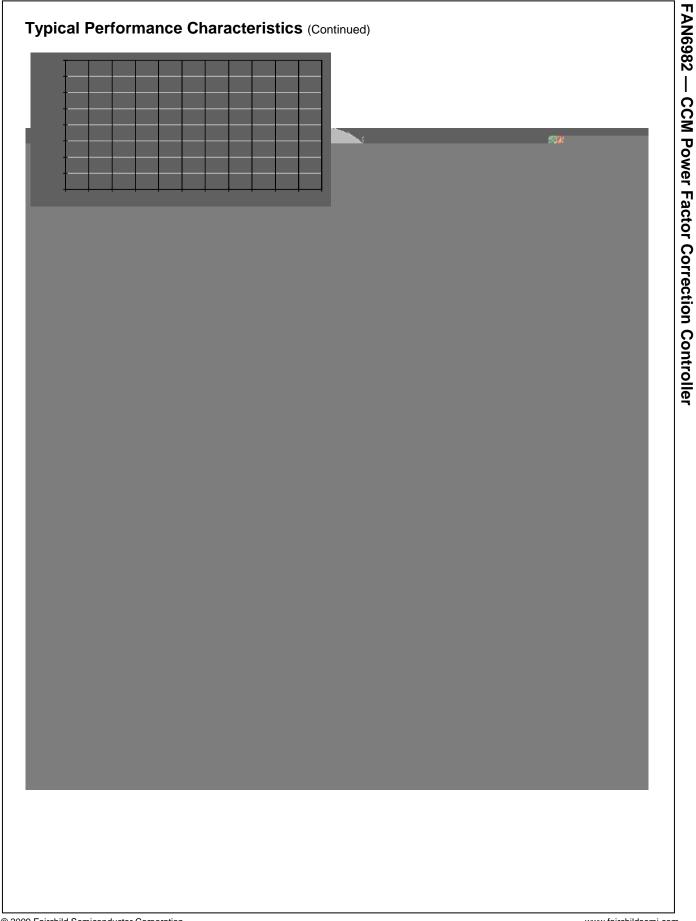


Symbol	Parameter	Conditions	Min.	Тур.	Max.	Units
oltage Erro	or Amplifier		1			1
V <sub>REF</sub>	Reference Voltage		2.45	2.50	2.55	V
Av	Open-Loop Gain <sup>(3)</sup>	At T <sub>A</sub> =25°C	35	42		dB
$Gm_V$	Transconductance	$V_{NONINV}=V_{INV}, V_{VEA}=3.75V \text{ at } T_A=25^{\circ}C$	50	70	90	µmho
I <sub>FBPFC-L</sub>	Maximum Source Current	V <sub>FBPFC</sub> =2V, V <sub>VEA</sub> =1.5V	40	50		μA
I <sub>FBPFC-H</sub> I <sub>BS</sub>	Maximum Sink Current	V <sub>FBPFC</sub> =3V, V <sub>VEA</sub> =6V	ļ	-50	-40	μA





mance Characteristics	Typical Performance Characteristics	FAN6982 — CCN	CCM Power Factor Correction Controller
rmance Characteristics	Typical Performance Characteristics		
	Typical Performance Characteristics		
rmance Charac	Typical Performance Charac	teristics	
	Typical Perform	nance Charact	



## **Functional Description**

## Oscillator

The internal oscillator frequency of FAN6982 is determined by the timing resistor and capacitor on the RT/CT pin, but note that the optimum operation for FAN6982 is between 50 and 75kHz. The frequency of the internal oscillator is given by:

$$f_{osc} = \frac{1}{0.56 \cdot R_T \cdot C_T + 360C_T}$$
(1)

The dead time for the PFC gate drive signal is determined by

$$t_{DEAD} = 360C_T \tag{2}$$

The dead time should be smaller than 2% of switching period to minimize line current distortion around line zero crossing.

## Gain Modulator

Gain modulator is the key block for PFC stage because it provides the reference to the current control error amplifier for the input current shaping, as shown in Figure 23. The output current of gain modulator is a function of  $V_{EA}$ ,  $I_{AC}$  and  $V_{RMS}$ . The gain of the gain modulator is given as a ratio between  $I_{MO}$  and  $I_{AC}$  with a given  $V_{RMS}$  when  $V_{EA}$  is saturated to high. The gain is inversely proportional to  $V_{RMS}^2$ , as shown in Figure 24, to implement line feed-forward. This automatically adjusts the reference of current control error amplifier according to the line voltage such that the input power of PFC converter is not changed with line voltage, as shown in, Figure 25. 8

The rectified sinusoidal signal is obtained by the current flowing into the IAC pin. The resistor  $R_{IAC}$  should be large enough to prevent saturation of the gain modulator as:

$$\frac{\sqrt{2}V_{LINE,BO}}{R_{IAC}} \cdot G^{MAX} < 159 \mu A \tag{3}$$

where  $V_{\text{LINE,BO}}$  is the line voltage that trips brownout protection,  $G^{MAX}$  is the maximum modulator gain when  $V_{\text{RMS}}$  is 1.08V, and 159µA is the maximum output current of the gain modulator.

## **Current-Control of Boost Stage**

As shown in Figure 27 the FAN6982 employs two control loops for power factor correction, a currentcontrol loop and a voltage-control loop. The currentcontrol loop shapes inductor current, as shown in Figure 28, based on the reference signal obtained at IAC pin as:

57) 76.7M0.963.n $I_{E} \otimes R_{CS1} = I_{MO} \cdot R_{M} = I_{AC} \cdot G \cdot R_{M}$ 

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