

FAN6248HC/HD/LC/LD

FAN6248HC/HD/LC/LD

PIN DESCRIPTION

Pin Number	Pin Name	Description
1	GATE1	Gate drive output for SR1
2	GND	Ground
3	VD1	Synchronous rectifier drain sense input. A $I_{OFFSET1}$ current source flows out of the DRAIN pin such that an external series resistor can be used to adjust the synchronous rectifier turn-off threshold. The $I_{OFFSET1}$ current source is turned off when V_{DD} is under-voltage or when switching is disabled in green mode
4	VS1	Synchronous rectifier source sense input for SR1
5	VS2	Synchronous rectifier source sense input for SR2
6	VD2	Synchronous rectifier drain sense input. A $I_{OFFSET2}$ current source flows out of the DRAIN pin such that an external series resistor can be used to adjust the synchronous rectifier turn-off threshold. The $I_{OFFSET2}$ current source is turned off when V_{DD} is under-voltage or when switching is disabled in green mode
7	VDD	Supply Voltage
8	GATE2	Gate drive output for SR2

ORDERING AND SHIPPING INFORMATION

Ordering Code	Device Marking	$V_{TH_OFF1} / V_{TH_OFF2}$	Package	Shipping [†]
FAN6248HCMX	FAN6248HC	25 mV / 50 mV	SOIC-8	2500 / Tape & Reel
FAN6248HDMX	FAN6248HD	0 mV / 25 mV	SOIC-8	2500 / Tape & Reel
FAN6248LCMX	FAN6248LC	25 mV / 50 mV	SOIC-8	2500 / Tape & Reel
FAN6248LDMX	FAN6248LD	0 mV / 25 mV	SOIC-8	2500 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel

FAN6248HC/HD/LC/LD

MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Unit
V_{DD}	Power Supply Input Pin Voltage	-0.3	30	V
V_{D1}, V_{D2}	Drain Sense Input Pin Voltage	-1	100	V
$V_{GATE1},$ V_{GATE2}				

FAN6248HC/HD/LC/LD

ELECTRICAL CHARACTERISTICS ($V_{DD} = 12\text{ V}$ and $T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
INPUT VOLTAGE						
V_{DD_ON}	Turn-On Threshold	V_{DD} rising	4.2	4.5		

FAN6248HC/HD/LC/LD

ELECTRICAL CHARACTERISTICS ($V_{DD} = 12\text{ V}$ and $T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$ unless otherwise specified) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
--------	-----------	------------	-----	-----	-----	------

MINIMUM ON-TIME AND MAXIMUM ON-TIME

$t_{ON_MIN_LL}^*$	Minimum On-Time Lower Limit for LC and LD version	$t_{ON_MIN_LL} < t_{ON_MIN} < t_{ON_MIN_UL}$		0.4		s
$t_{ON_MIN_UL}$	Minimum On-Time Upper Limit for LD and LD version		3.2	4	4.8	s
$t_{SR_CNDT_H}$	Minimum SR Conduction Time to enable SR for HC and HD version	The duration from turn-on trigger to V_{DS} rising above V_{TH_HGH}	380	600	820	ns
$t_{SR_CNDT_L}$	Minimum SR Conduction Time to enable SR for LC and LD version	The duration from turn-on trigger to V_{DS} rising above V_{TH_HGH}	0.85	1.2	1.65	s
$t_{SR_MAX_H}^*$	Maximum SR Turn-on Time for HC and HD version			15		s
$t_{SR_MAX_L}^*$	Maximum SR Turn-on Time for LC and LD version			30		s

REGULATED DEAD TIME

$t_{DEAD_H}^*$	Dead time regulation target for HC and HD version	From V_{GATE} falling below V_{G_LW} to V_{DS} rising above V_{TH_HGH}		280		ns
$t_{DEAD_H_LIGHT}^*$	Dead time regulation target under light load condition for HC and HD version	From V_{GATE} falling below V_{G_LW} to V_{DS} rising above V_{TH_HGH}		320		ns
$t_{DEAD_L}^*$	Dead time regulation target for LC and LD version	From V_{GATE} falling below V_{G_LW} to V_{DS} rising above V_{TH_HGH}		320		ns
$t_{DEAD_L_LIGHT}^*$	Dead time regulation target under light load condition for LC and LD version	From V_{GATE} falling below V_{G_LW} to V_{DS} rising above V_{TH_HGH}		360		ns
t_{TSDT}^*	Too small dead time threshold to speed up I_{OFFSET} change (Speed up 2 times)	From V_{GATE} falling below V_{G_LW} to V_{DS} rising above V_{TH_HGH}		50		ns
K_{INV}^*	Adaptive SR current inversion detection time Ratio between T_{INV} and SR conduction time of previous switching cycle	$V_{GATE} > V_{G_HG}$ and $V_{DS} > V_{TH_OFF}$ $K_{INV} = 0.25 \times K_{TON}$		6.25		%
INV_EXT^*	Normal switching cycles without capacitive current spike to exit SR current inversion detection state which has t_{ON_DLY2}			31		cycle

GREEN MODE CONTROL

$t_{GRN_ENT_H}$	Non-Switching Period to Enter Green Mode for HC and HD version	Non switching cycles between burst switching bundles	60	80	100	s
$t_{GRN_ENT_L}$						

FAN6248HC/HD/LC/LD

ELECTRICAL CHARACTERISTICS ($V_{DD} = 12\text{ V}$ and $T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$ unless otherwise specified) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
--------	-----------	------------	-----	-----	-----	------

GREEN MODE CONTROL

$t_{S_NORMAL_H}$	Switching period to be recognized as normal switching for HC and HD version		13	20	27	s
$t_{S_NORMAL_L}$	Switching period to be recognized as normal switching for LC and LD version		27	40	53	s

OUTPUT DRIVER SECTION

V_{GATE_MAX}	Gate Clamping Voltage	$12\text{ V} < V_{DD} < 25\text{ V}$	9	10.5	12	V
V_{OL}	Output Voltage Low	$V_{DD} = 12\text{ V}, V_{D1} = V_{D2}$				

FAN6248HC/HD/LC/LD

TYPICAL CHARACTERISTICS



Figure 3. V_{DD_ON}



Figure 4. V_{DD_OFF}

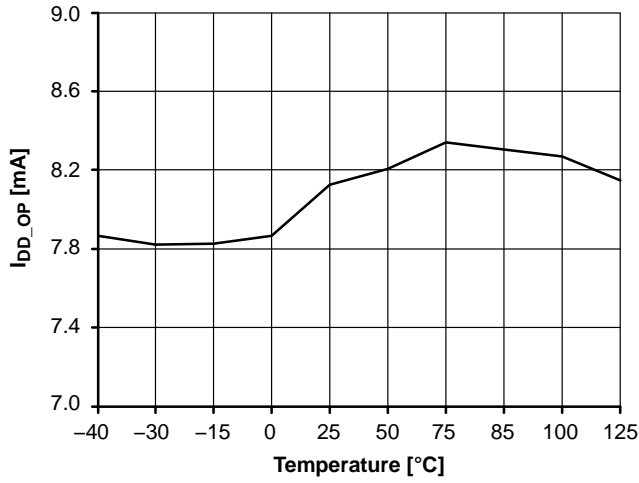


Figure 5. I_{DD_OP}



Figure 6. I_{DD_GREEN}

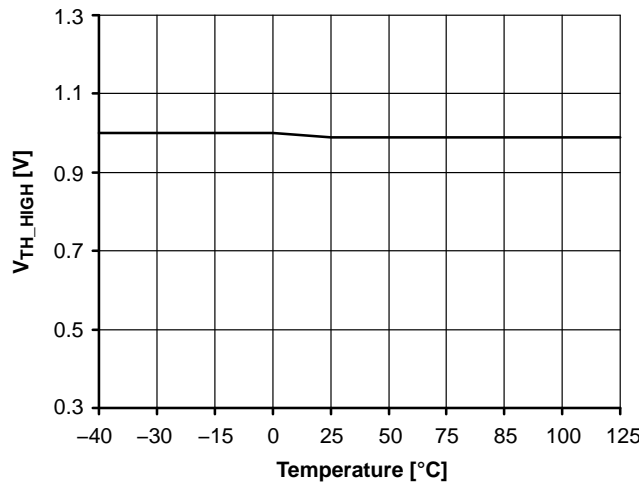


Figure 7. V_{TH_HIGH}

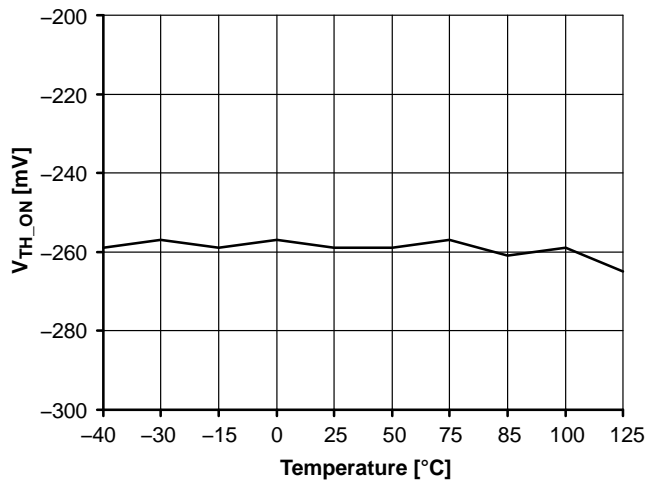


Figure 8. V_{TH_ON}

FAN6248HC/HD/LC/LD

TYPICAL CHARACTERISTICS

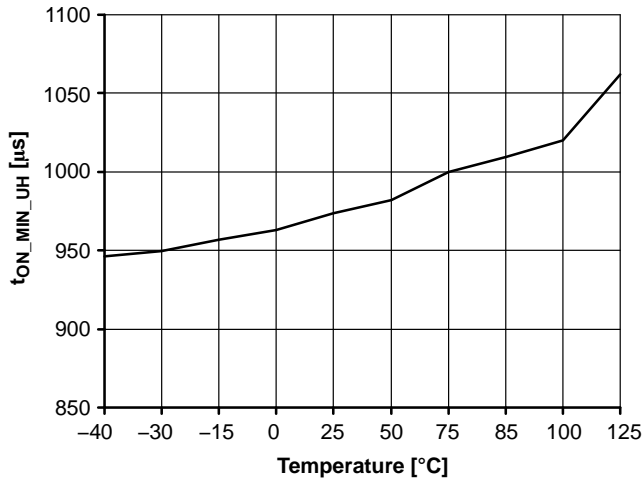


Figure 9. tON_DLY2_H

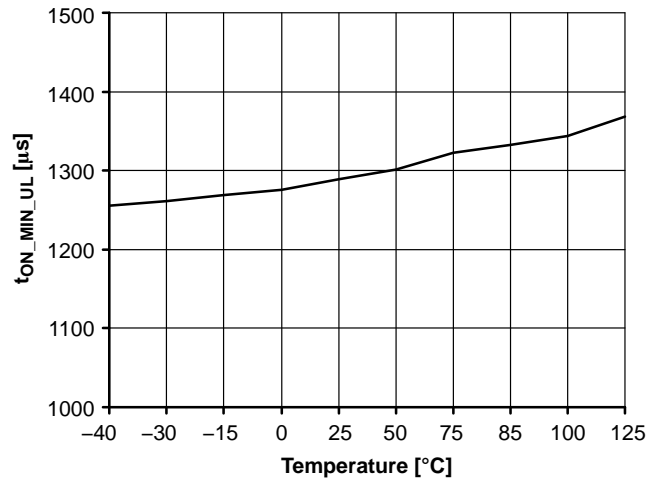


Figure 10. tON_DLY2_L

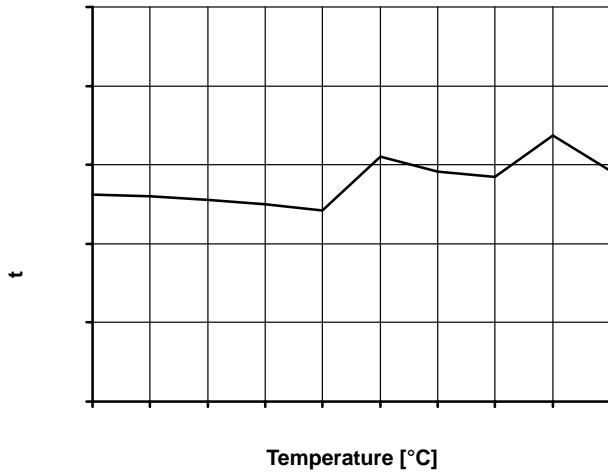


Figure 11. tSR_CNDT_H

Figure 12. tSR_CNDT_L

Figure 13. tGRN_ENT_H

Figure 14. tGRN_ENT_L

APPLICATION INFORMATION

Basic Operation Principle

FAN6248 controls the SR MOSFET based on the instantaneous drain-to-source voltage sensed across *DRAIN* and *SOURCE* pins. Before SR gate is turned on, SR body diode operates as the conventional diode rectifier. Once the body diode starts conducting, the drain-to-source voltage drops below the turn-on threshold voltage V_{TH_ON} which triggers the turn-on of the SR gate. Then the drain-to-source voltage is determined by the product of turn-on resistance R_{ds_on} of SR MOSFET and instantaneous SR current. When the drain-to-source voltage reaches the turn-off threshold voltage V_{TH_OFF} as SR MOSFET current decreases to near zero, FAN6248 turns off the gate. If a SR dead time is larger or smaller than the dead time regulation target t_{DEAD} , FAN6248 adaptively changes internal offset voltage to compensate the dead time. In addition, to prevent cross conduction SR operation, FAN6248 has 200 ns of turn-on blocking time just after alternating SR gate is turned off.

SR Turn-off Algorithm

Since a SR turn-off method determines SR conduction time and stable SR operation, the SR turn-off method is one of important feature of SR controllers. The SR turn-off method can be classified into two methods. The first method uses present information by an instantaneous drain voltage. This method is widely used and easy to realize, and can prevent late turn-off. However, it may show premature turn-off by parasitic stray inductances caused by PCB pattern and lead frame of SR MOSFET. The second method predicts SR conduction time by using previous cycle drain voltage information. Since it can prevent the premature turn-off, it is good for the system with constant operating frequency and turn-on time. However, in case of the frequency varying system, it may lead late turn-off so that negative current can flow in the secondary side.

To achieve both advantages, FAN6248 adopts mixed type control method as shown in Figure 21. Basically the instantaneous drain voltage V_{Drain} is compared with V_{TH_OFF} to turn off SR gate. Then, the offset voltage V_{offset} , which is determined by the product R_{offset} and I_{offset} , is added to V_{Drain} in order to compensate the stray inductance effect and maintain 280 ns of t_{DEAD} regardless of parasitic inductances. R_{offset} is an external resistor in Figure 1 and I_{offset} is an internal modulation current in Figure 2. Therefore, FAN6248 can show robust operation with minimum dead time.

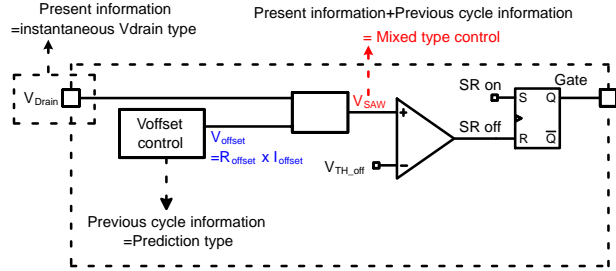


Figure 21. SR Turn-off Algorithm

Adaptive Dead Time Control

The stray inductances of the lead frame of SR MOSFET and PCB pattern induce positive voltage offset across drain-to-source voltage when SR current decreases. This

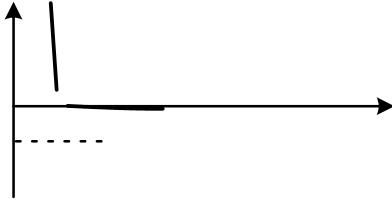


Figure 23. Premature SR Gate Turn-off
($T_{DEAD} > t_{DEAD_H}$)

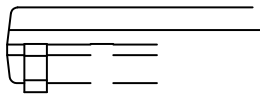
Light Load Detection (LLD)

To guarantee stable operation under light load condition, FAN6248 adopts a light load detection function. The modulation current I_{OFFSET} is mainly used for the adaptive dead time control. When the output load is heavy, I_{OFFSET_STEP} declines due to large di/dt in the secondary side current to maintain 280 ns of t_{DEAD} in FAN6248HC(D). On the contrary, I_{OFFSET_STEP} increases at light load condition by

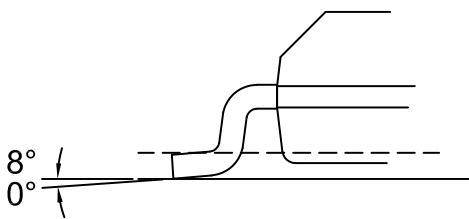
SOIC8
CASE 751EB
ISSUE A

DATE 24 AUG 2017

SEE DE



7



onsemi, **onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi**
