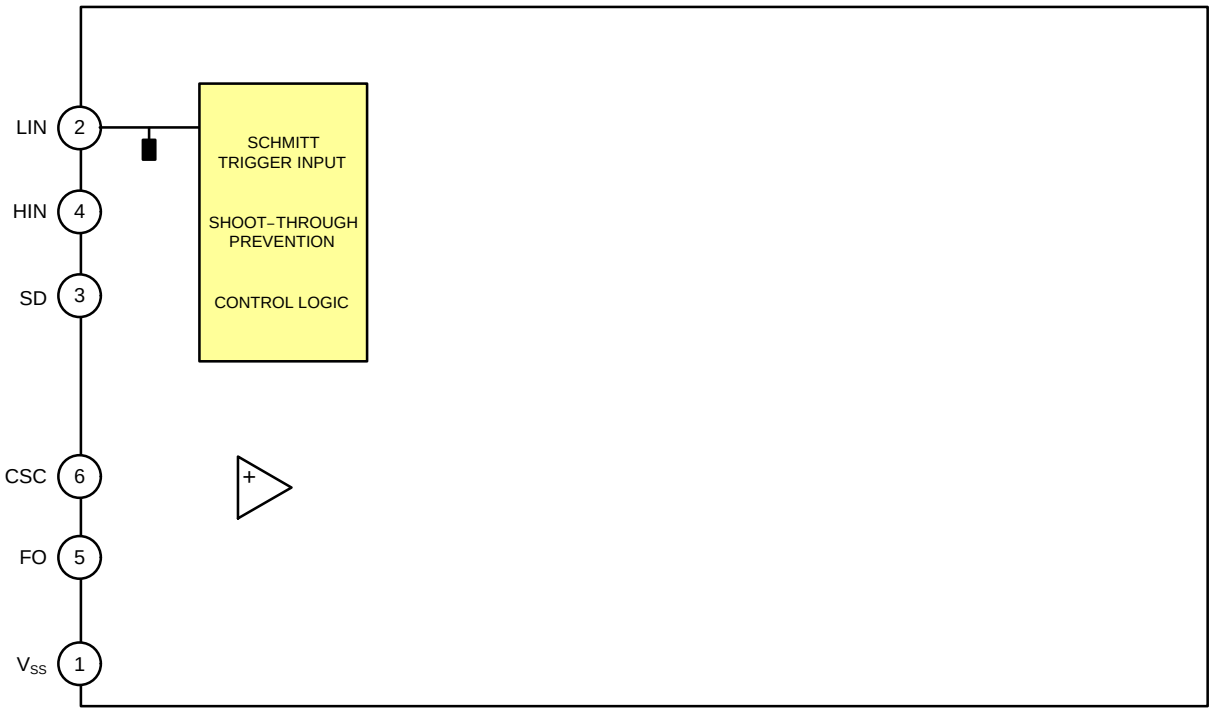
## BLOCK DIAGRAM



## SPECIFICATIONS

**ABSOLUTE MAXIMUM RATINGS** ($T_A$ = 25 C, unless otherwise specified.)

| Symbol | Rating | Value | Unit |
|---|---|---|---|
| $V_S$ | High−side Offset Voltage $V_S$ | ($V_B$ − 25) to ($V_B$ + 0.3) | V |
| $V_B$ | High−side Floating Supply Voltage $V_B$ | −0.3 to 1225 | V |
| $V_{HO}$ | High−side Floating Output Voltage | ($V_S$ – 0.3) to ($V_B$ + 0.3) | V |
| $V_{DD}$ | Low−side and Logic−fixed Supply Voltage | −0.3 to 25 | V |
| $V_{IN}$ | Logic Input Voltage (HIN, LIN, $\overline{SD}$) | −0.3 to ($V_{DD}$ + 0.3) | V |
| $V_{CSC}$ | Current Sense Input Voltage | −0.3 to ($V_{DD}$ + 0.3) | V |
| $dV_S/dt$ | Allowable Offset Voltage Slew Rate | 50 | V/ns |
| $P_D$ | Power Dissipation (SO14NB) (Note 1) | 0.8 | W |
| JA | Thermal Resistance, Junction−to−Ambient (SO14NB) | 156 | C/W |
| $T_{J(max)}$ | Junction Temperature | +150 | C |
| TSTG | Storage Temperature | −55 to +150 | C |
| ESDHBM | ESD, Human Body Model (Note 3) | 2500 | V |
| ESDCDM | ESD, Charged Device Model (Note 3) | 750 | V |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Do not exceed PD under any circumstances.
2. Mounted on 76.2 114.3 1.6 mm PCB (FR−4 glass epoxy material). Refer to the following standards:
   - JESD51−2: Integral circuits thermal test method environmental conditions – natural convection
   - JESD51−3: Low effective thermal conductivity test board for leaded surface mount packages
3. This device series incorporates ESD protection and is tested by the following methods:
   - ESD Human Body Model tested per ANSI/ESDA/JEDEC JS−001−2012
   - ESD Charged Device Model tested per JESD22−C101

**RECOMMENDED OPERATING RANGES** (Parameters are referenced to $V_{SS}$)

| Symbol | Rating | Min | Max | Unit |
|---|---|---|---|---|
| $V_{DD}$ | Supply Voltage Range | 4.5 | 18.0 | V |
| $V_S$ | High−Side $V_S$ Floating Supply Offset Voltage (Note 4) | 5 − $V_{BS}$ | 1200 | V |
| $V_{BS}$ | High−side $V_{BS}$ Bootstrap Voltage | $V_{BSUV+}$ | 22 | V |
| $V_{HO}$ | High−Side Output Voltage | $V_S$ | $V_B$ | V |
| $V_{DD}$ | Low−Side and Logic Supply Voltage | $V_{DDUV+}$ | 22 | V |
| $V_h$ | | | | |

**ELECTRICAL CHARACTERISTICS**

($V_{BIAS}$ ($V_{DD}$, $V_{BS}$) = 15 V, $T_A$ = −40 C to 125 C unless otherwise specified. The $V_{IN}$ and $I_{IN}$ parameters are referenced to V

**ELECTRICAL CHARACTERISTICS** (continued)
($V_{BIAS}$ ($V_{DD}$, $V_{BS}$) = 15 V, $T_A$ = −40 C to 125 C unless otherwise specified. The $V_{IN}$ and $I_{IN}$ parameters are referenced to $V_{SS}$. The $V_O$ and $I_O$ parameters are referenced to $V_S$ and COM and are applicable to the respective outputs HO and LO.)

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **FAULT DETECTION SECTION** | | | | | | |
| $V_{FOH}$ | Fault Output High Level Voltage | $V_{CSC}$ = 0 V, $R_{PULL-UP}$ = 4.7 kΩ | 4.7 | – | – | V |
| $V_{FOL}$ | Fault Output Low Level Voltage | $V_{CSC}$ = 1 V, $I_{FO}$ = 2 mA | – | – | 0.8 | V |

**DYNAMIC OUTPUT SECTION**
($V_{BIAS}$ ($V_{DD}$, $V_{BS}$) = 15.0 V, $T_A$ = −40 C to 125

## TYPICAL CHARACTERISTICS (Continued)

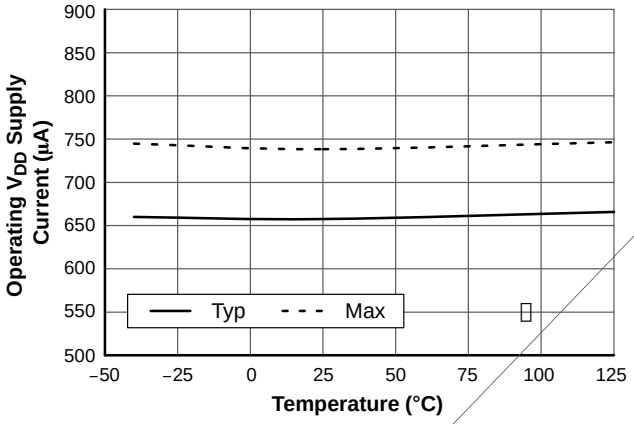



**Figure 10. $V_{DD}$ Operating Current vs. Temperature**

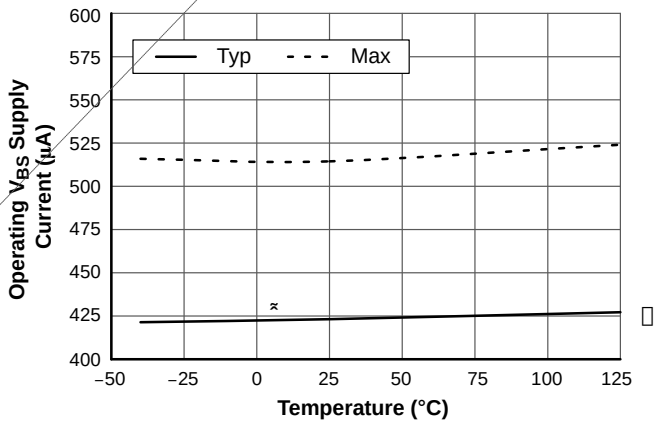



**Figure 11. $V_{BS}$ Operating Current vs. Temperature**

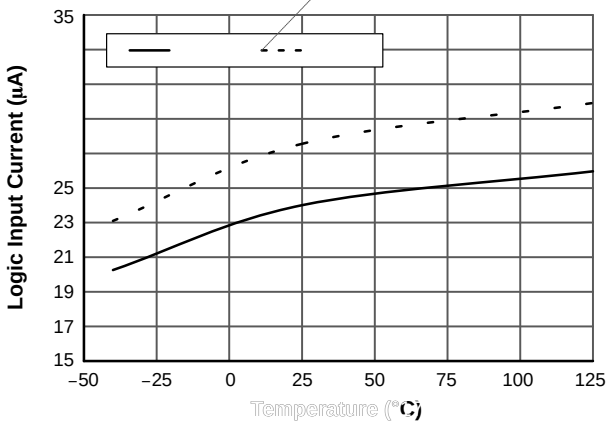



**Figure 12. Logic High Input Bias Current vs. Temperature**

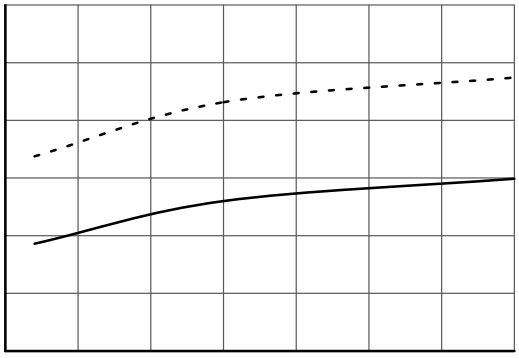


**Figure 13. $I_{CSCIN}$ vs. Temperature**

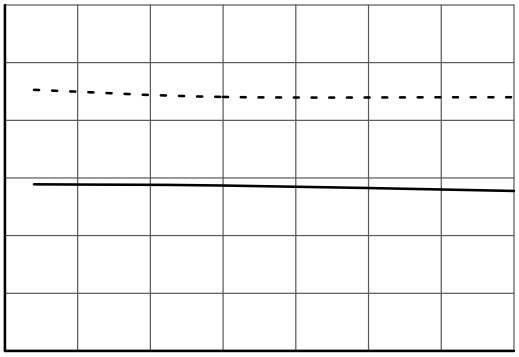


**Figure 14. $I_{SOFT}$ vs. Temperature**

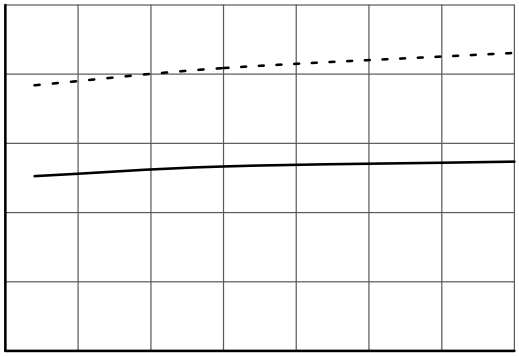
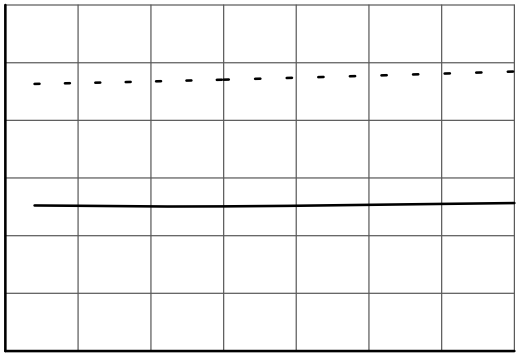
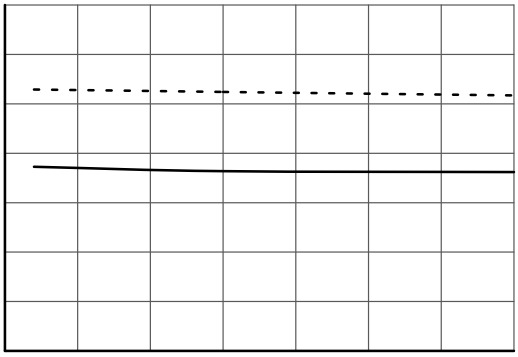
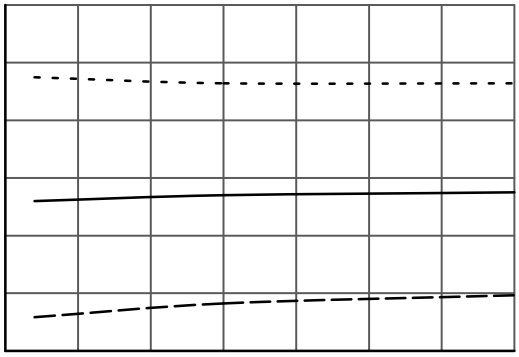


**Figure 15. Turn−on Rising Time vs. Temperature**

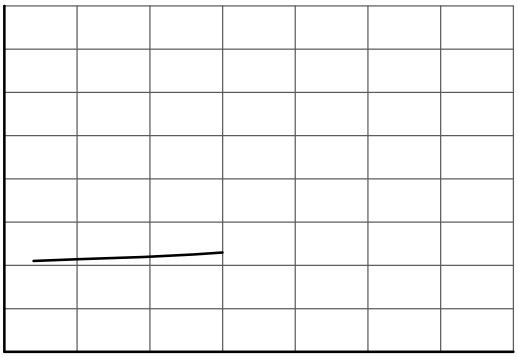
## TYPICAL CHARACTERISTICS (Continued)

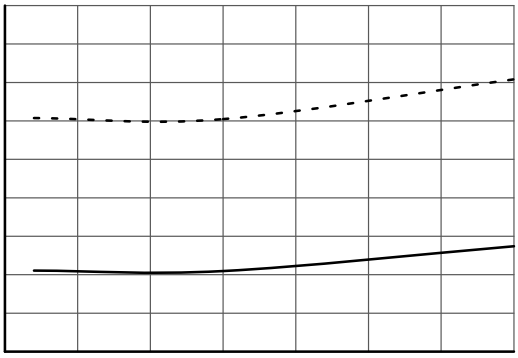


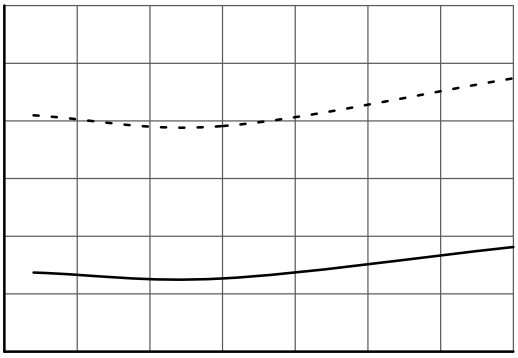


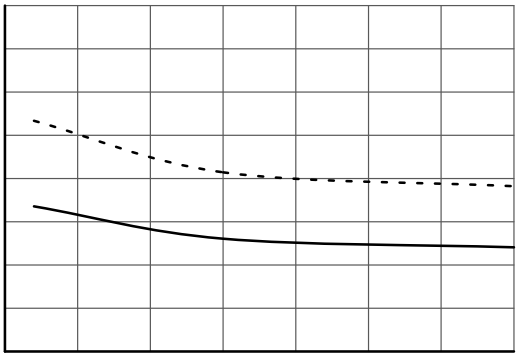


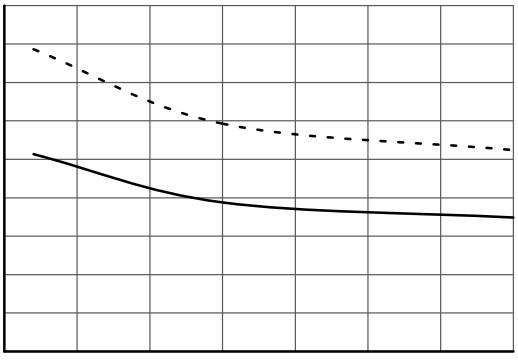
## TYPICAL CHARACTERISTICS (Continued)











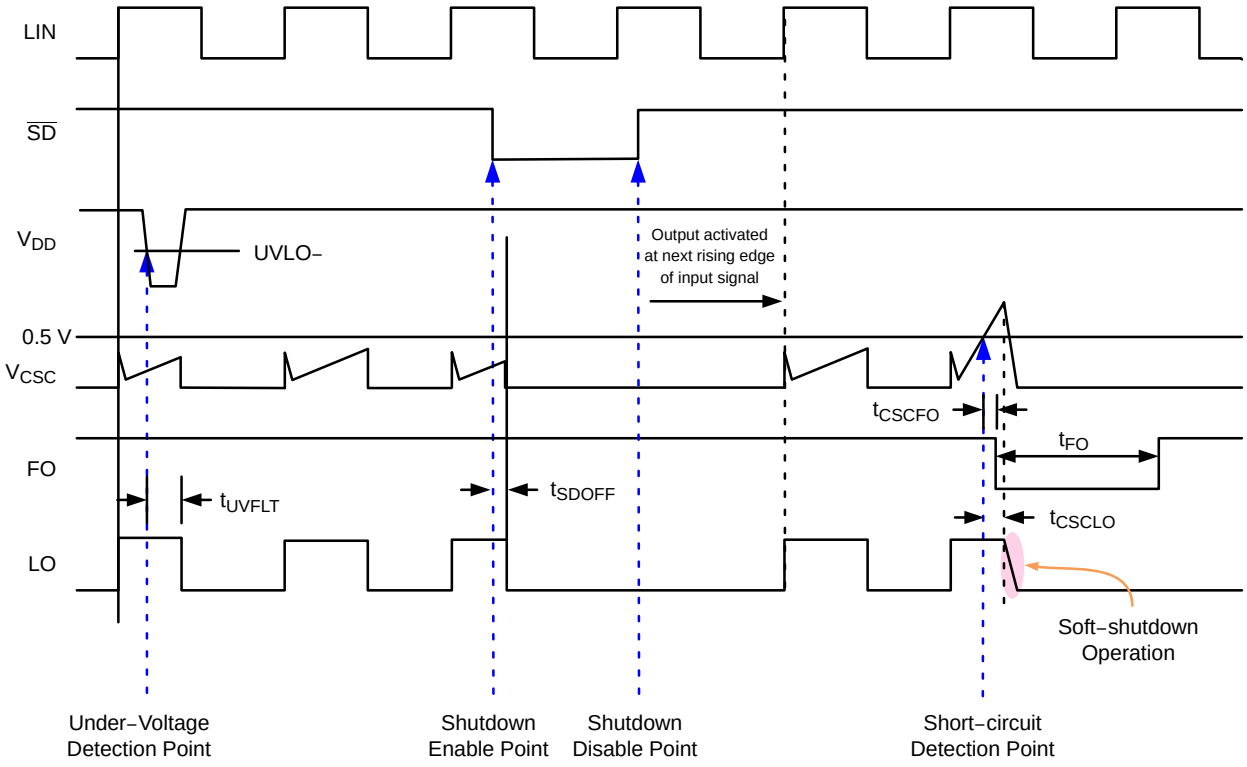



**Figure 42. Switching Timing Waveforms Definition – Low Side**

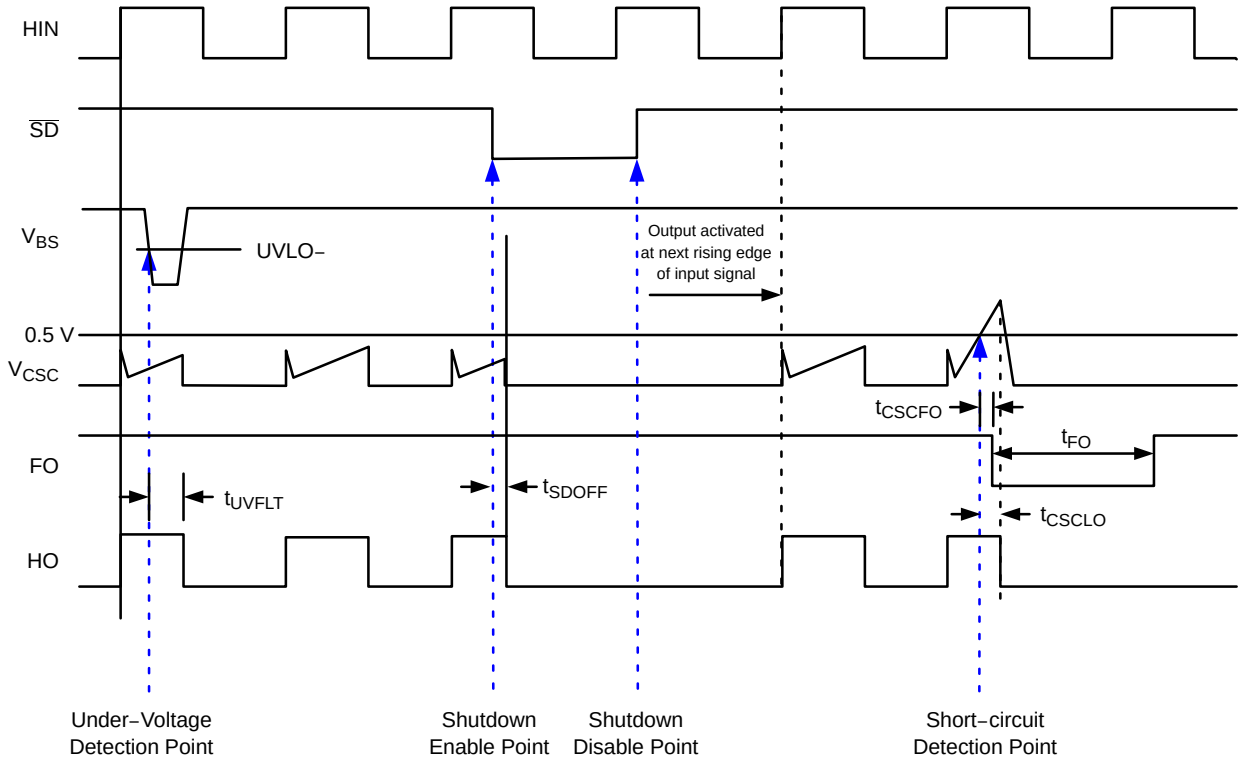
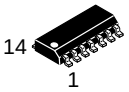



**Figure 43. Switching Timing Waveforms Definition – High Side**




**SCALE 1:1**

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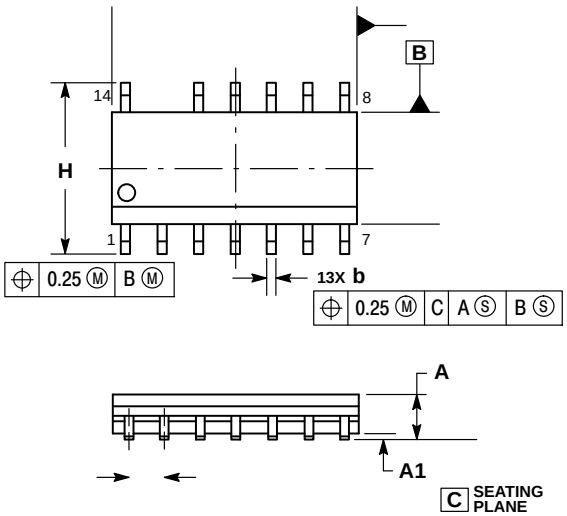
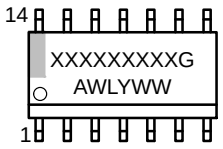



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

**GENERIC**
**MARKING DIAGRAM***




XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

**STYLES ON PAGE 2**

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STYLE 7:
PIN 1. ANODE/CATHODE
2. COMMON ANODE
3. COMMON CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE