

# FAD6263

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*Product Preview*

**Half-Bridge Gate Driver,**

**600 V, 3 A Half-Bridge for**

- Under Voltage LockOut (UVLO) for Both Channels
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FAD6263

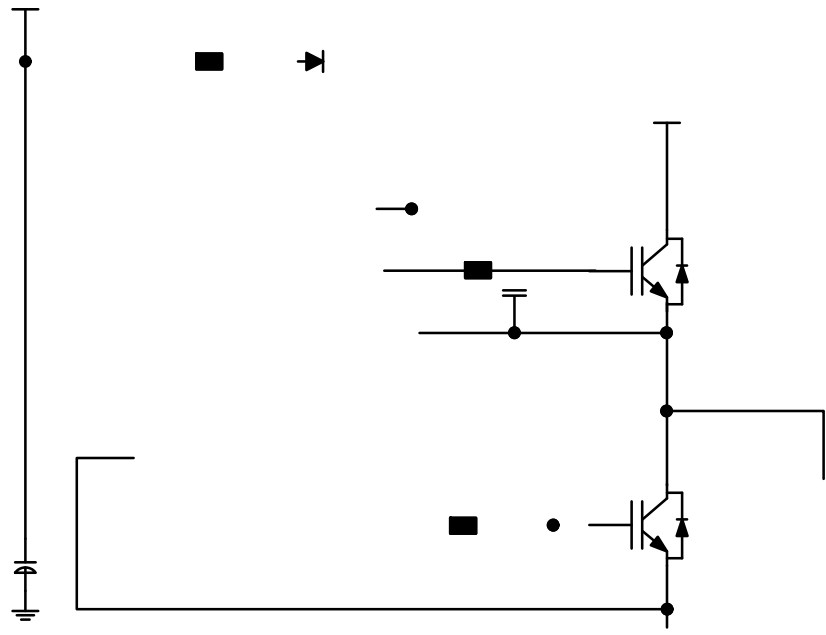
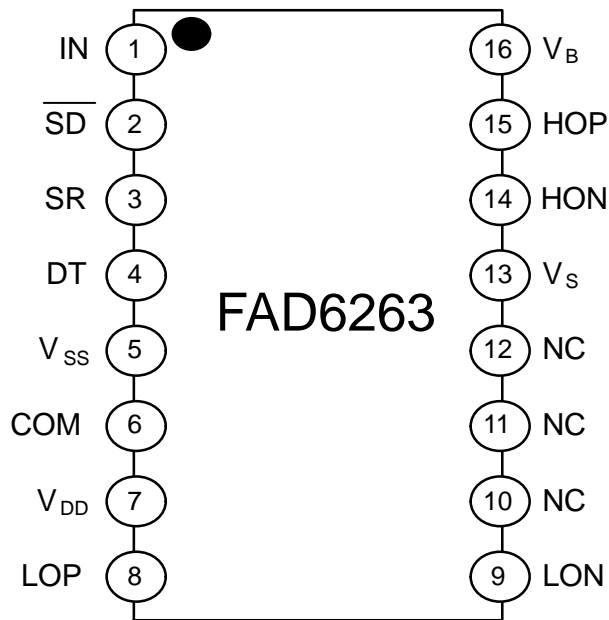


Figure 1. Application Schematic – SOIC16

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**Figure 3. Pin Connection (Top View)**

**Table 1. PIN FUNCTION DESCRIPTION**

Pin Number	Pin Name	Description
1	IN	Logic Input for Complementary Outputs
2	$\overline{SD}$	Logic Input Shutdown (Active Low)
3	SR	Shutdown Reset
4	DT	Dead Time Control with External Resistor (referenced to VSS)
5	VSS	Logic Ground
6	COM	Power Ground, Low Side Driver Return
7	VDD	Low Side and Logic Power Supply Voltage
8	LOP	Low Side Driver Output (Pull Up)
9	LON	Low Side Driver Output (Pull Down)
10	NC	No Electrical Connection (Note 1)
11	NC	No Electrical Connection (Note 1)
12	NC	No Electrical Connection (Note 1)
13	VS	

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**Table 2. MAXIMUM RATINGS**

Rating	Symbol	Value	Unit
High Side Floating Supply Voltage	$V_B$	0.3 to 625	

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**Table 4. ELECTRICAL CHARACTERISTICS**

$V_{BIAS}$  ( $V_{DD}$ ,  $V_{BS}$ ) = 15 V,  $V_{SS}$  = COM = 0 V,  $DT = V_{SS}$  and  $T_A = 40^\circ\text{C}$  to  $125^\circ\text{C}$  unless otherwise noted.)

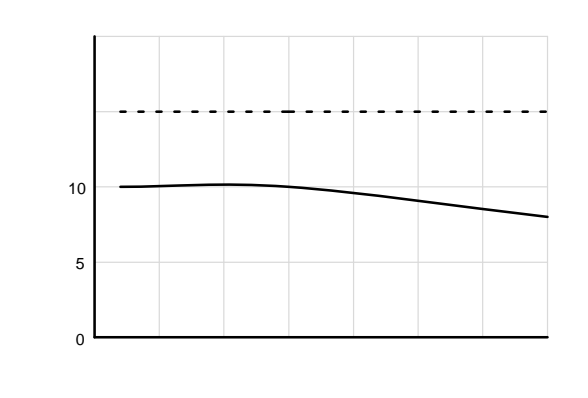
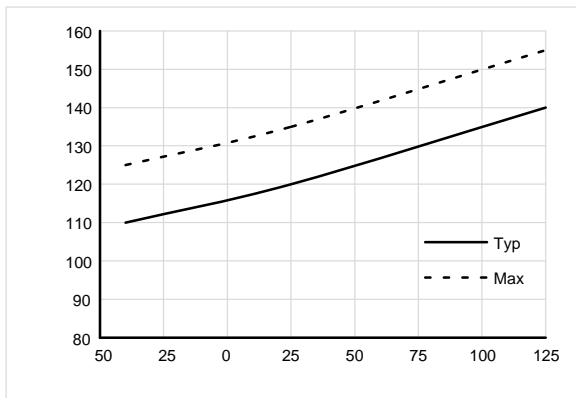
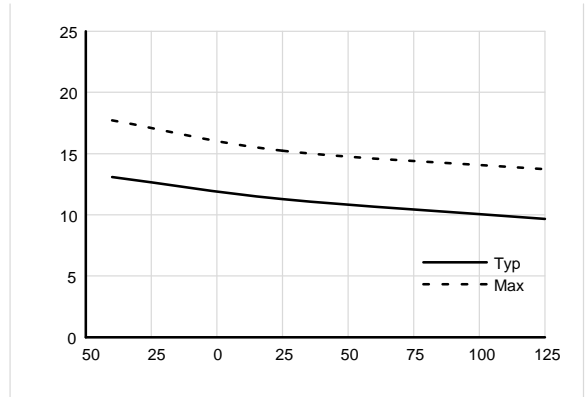
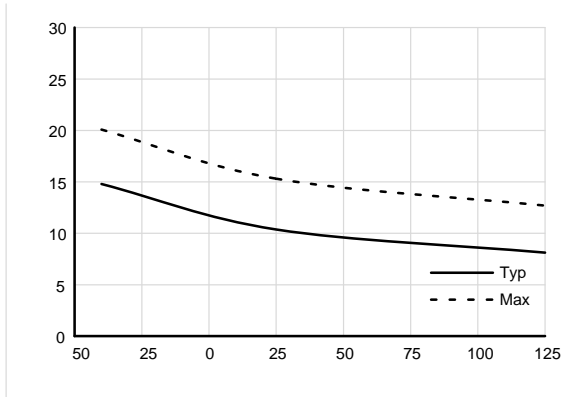
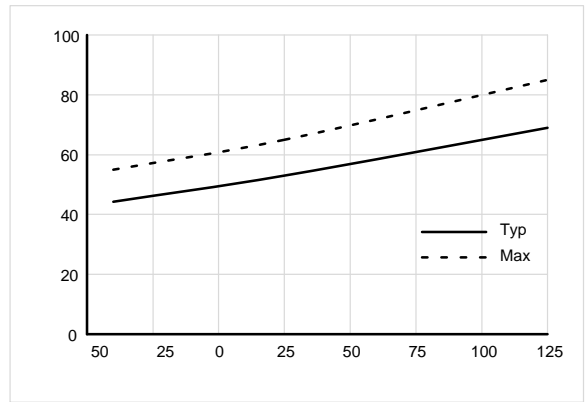
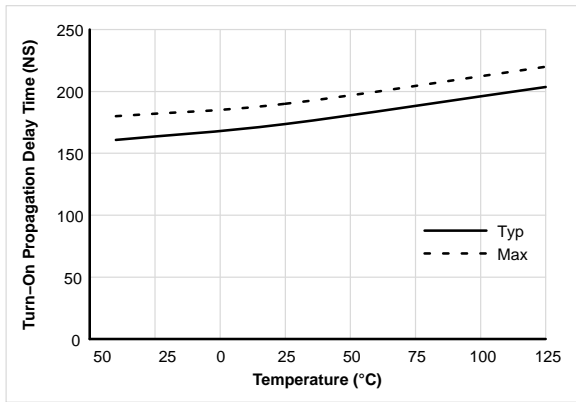
Parameter	Test Condition	Symbol	Min	Typ	Max	Unit
<b>POWER SUPPLY SECTION (<math>V_{DD}</math> and <math>V_{BS}</math>)</b>						
$V_{DD}$ and $V_{BS}$ Supply Under Voltage Positive going Threshold		$V_{DDUV+}$ $V_{BSUV+}$	7.3	8.3	9.3	V
$V_{DD}$ and $V_{BS}$ Supply Under Voltage Negative going Threshold		$V_{DDUV}$ $V_{BSUV}$	6.7	7.8	8.6	
$V_{DD}$ and $V_{BS}$ Supply Under Voltage Lockout Hysteresis Voltage		$V_{DDUVH}$ $V_{BSUVH}$		0.5		
Offset Supply Leakage Current	$V_B = V_S = 600$ V	$I_{LK}$			50	$\mu\text{A}$
Quiescent $V_{DD}$ Supply Current	$V_{IN} = 0$ V or 5 V	$I_{QDD}$		355	550	
Quiescent $V_{BS}$ Supply Current	$V_{IN} = 0$ V or 5 V	$I_{QBS}$		45	110	
Operating $V_{DD}$ Supply Current	$V_{IN} = 0$ to 5 V; $f_{SW} = 20$ kHz; $C_L = 1$ nF	$I_{PDDSW}$				

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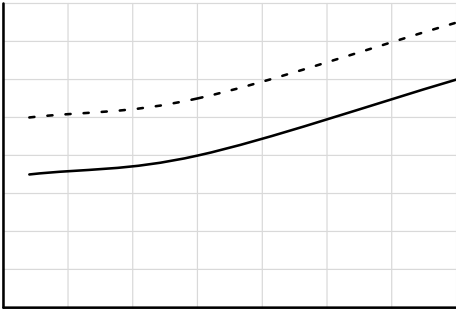
## Table 4. ELECTRICAL CHARACTERISTICS

$V_{BIAS}$  ( $V_{DD}$ ,  $V_{BS}$ ) = 15 V,  $V_{SS}$  = COM = 0 V, DT =  $V_{SS}$  and  $T_A$  = C (C unless otherwise noted.)

TYPICAL PERFORMANCE CHARACTERISTICS



TYPICAL PERFORMANCE CHARACTERISTICS (Continued)





TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

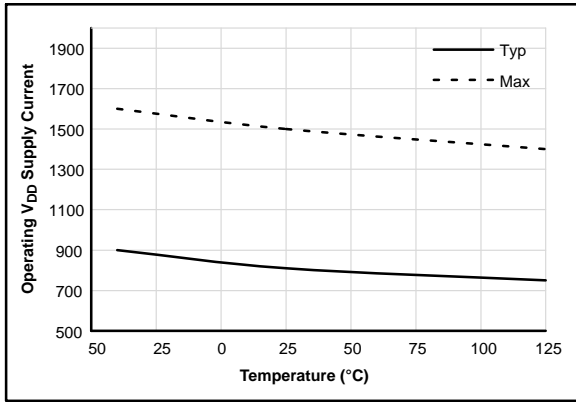


Figure 16. Operating  $V_{DD}$  Supply Current vs. Temperature

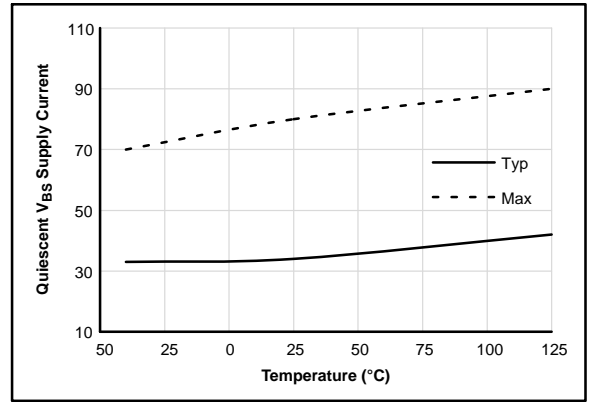


Figure 17. Quiescent  $V_{BS}$  Supply Current vs. Temperature

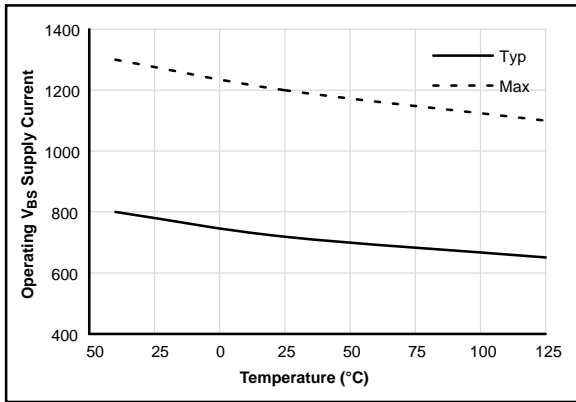


Figure 18. Operating  $V_{BS}$  Supply Current vs. Temperature

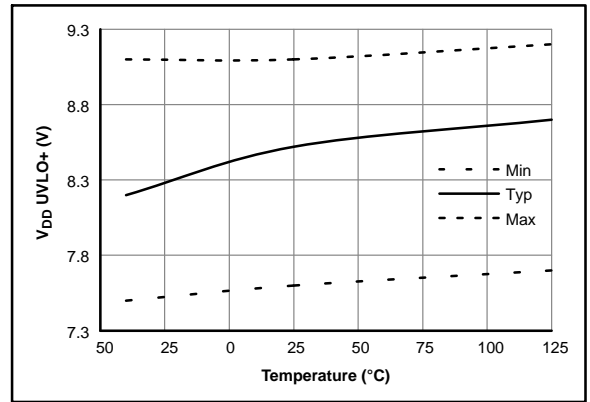


Figure 19.  $V_{DD}$  UVLO+ vs. Temperature

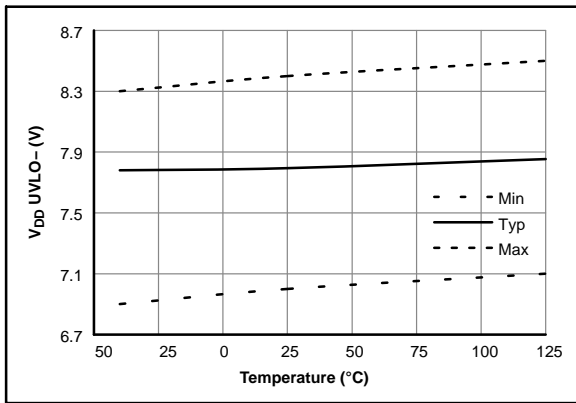


Figure 20.  $V_{DD}$  UVLO- vs. Temperature

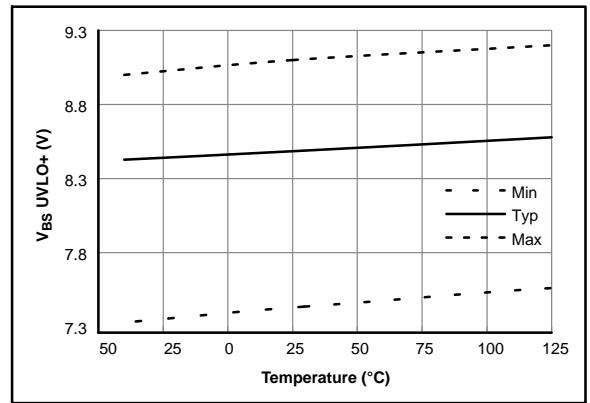
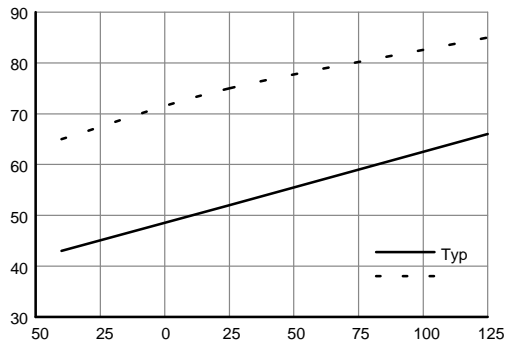
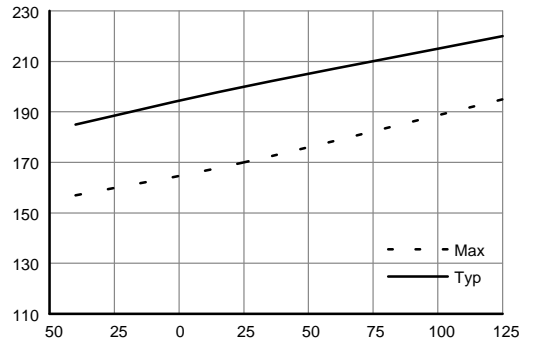
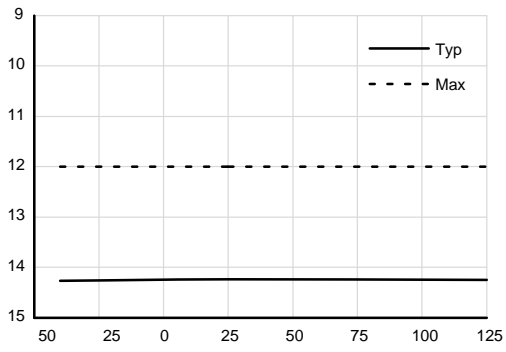


Figure 21.  $V_{BS}$  UVLO+ vs. Temperature

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## TYPICAL PERFORMANCE CHARACTERISTICS (Continued)



TOFF (ns)

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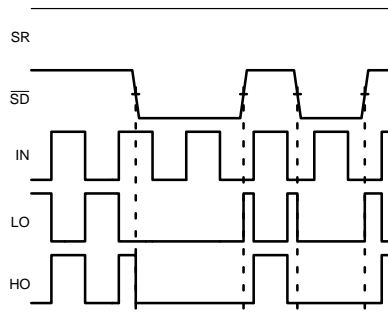
## APPLICATIONS DESCRIPTION

### Power On Reset (POR) Sequence

The purpose of the POR sequence is to ensure that the logic circuitry has reached a stable state after Vdd has ramped up before the gate driver can be operated:

1. Ramp up V

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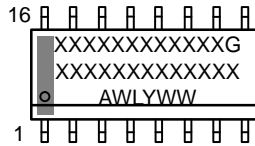


**SOIC-16 9.90x3.90x1.50 1.27P**  
CASE 751B  
ISSUE L

**SOIC-16 9.90x3.90x1.50 1.27P**  
**CASE 751B**  
**ISSUE L**

DATE 29 MAY 2024

**GENERIC  
MARKING DIAGRAM\***



XXXXX = Specific Device Code  
A = Assembly Location  
WL = Wafer Lot  
Y = Year  
WW = Work Week  
G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

<p>S 1: 1. C C ✓  2. BAS ✓  3. ✓  4. C C ✓  5. ✓  6. BAS ✓  7. C C ✓  8. C C ✓  9. BAS ✓  10. ✓  11. C C ✓  12. ✓  13. BAS ✓  14. C C ✓  15. ✓  16. C C ✓</p>	<p>S 2: 1. CA ✓  2. A ✓  3. C C ✓  4. CA ✓  5. CA ✓  6. C C ✓  7. A ✓  8. CA ✓  9. CA ✓  10. A ✓  11. C C ✓  12. CA ✓  13. CA ✓  14. C C ✓  15. A ✓  16. CA ✓</p>	<p>S 3: 1. C C , #1 ✓  2. BAS , #1 ✓  3. , #1 ✓  4. C C , #1 ✓  5. C C , #2 ✓  6. BAS , #2 ✓  7. , #2 ✓  8. C C , #2 ✓  9. C C , #3 ✓  10. BAS , #3 ✓  11. , #3 ✓  12. C C , #3 ✓  13. C C , #4 ✓  14. BAS , #4 ✓  15. , #4 ✓  16. C C , #4 ✓</p>	<p>S 4: 1. C C , #1 ✓  2. C C , #1 ✓  3. C C , #2 ✓  4. C C , #2 ✓  5. C C , #3 ✓  6. C C , #3 ✓  7. C C , #4 ✓  8. C C , #4 ✓  9. BAS , #4 ✓  10. , #4 ✓  11. BAS , #3 ✓  12. , #3 ✓  13. BAS , #2 ✓  14. , #2 ✓  15. BAS , #1 ✓  16. , #1 ✓</p>
<p>S 5: 1. A , #1 ✓  2. A , #1 ✓  3. A , #2 ✓  4. A , #2 ✓  5. A , #3 ✓  6. A , #3 ✓  7. A , #4 ✓  8. A , #4 ✓  9. A , #4 ✓  10. S C , #4 ✓  11. A , #3 ✓  12. S C , #3 ✓  13. A , #2 ✓  14. S C , #2 ✓  15. A , #1 ✓  16. S C , #1 ✓</p>	<p>S 6: 1. CA ✓  2. CA ✓  3. CA ✓  4. CA ✓  5. CA ✓  6. CA ✓  7. CA ✓  8. CA ✓  9. A ✓  10. A ✓  11. A ✓  12. A ✓  13. A ✓  14. A ✓  15. A ✓  16. A ✓</p>	<p>S 7: 1. S C -C ✓  2. C A ( ) ✓  3. C A ( ) ✓  4. A -C ✓  5. C A ( ) ✓  6. C A ( ) ✓  7. C A ( ) ✓  8. S C -C ✓  9. S C -C ✓  10. C A ( ) ✓  11. C A ( ) ✓  12. C A ( ) ✓  13. A -C ✓  14. C A ( ) ✓  15. C A ( ) ✓  16. S C -C ✓</p>	

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<b>DESCRIPTION:</b>	<b>SOIC-16 9.90X3.90X1.50 1.27P</b>	<b>PAGE 2 OF 2</b>

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