Audio Processor for Digital Hearing Aids

EZAIRO 8310 Hybrid

Introduction

Ezairo 8310 is an open-programmable DSP-based hybrid specifically designed for use in high-performance hearing aids and hearables. The Ezairo 8310 hybrid includes the Ezairo 8300 System-on-Chip (SoC), onsemi's high-end DSP processor, as well as the LE25S161 onsemi's ultra-low power flash memory.

Ezairo 8300 includes six programmable or semi-programmable processing cores, providing a high degree of parallelism and flexibility:

- The CFX is an open-programmable dual-Harvard 24 bits digital signal processor (DSP) providing support for any type of audio signal processing
- The Arm® Cortex®-M3 processor is a 32-bit RISC processor providing support for general processing and interfacing to external components
- The HEAR configurable accelerator core is optimized for pre-programmed functions that are frequently needed in audio signal processing
- The Filter Engine allows time domain filtering and supports an ultra-low-delay audio path
- The LPDSP32 is an open-programmable dual

KEY FEATURES

- High Performance: Best in class MIPS/mW.
- Programmable Flexibility: the open−programmable DSP−based

Table 1. ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Typ	Max	Unit	Notes
VBAT	ï	ï	1.98	V	Power supply voltage
VBATOD	ï	ï	1.98	V	Output driver power supply voltage
VDDO2/3	ï	ï	1.98	V	I/O supply voltage
VSSA	0	ï	ï	V	Analog ground
VSSOD	0	ï	ï	V	Output driver ground
VSSC					

Table 3. ELECTRICAL PERFORMANCE SPECIFICATIONS

Unless otherwise noted, the specifications mentioned in the table below are valid at 25°C at VBAT = 1.25 V. The system clock (SYS_CLK) was set to 15.36 MHz. Parameters marked as screened are tested on each chip. Parameters marked as screened with one check are tested on each Ezairo 8300 chip and with two checks are tested on each Ezairo 8310 hybrid module.

VDDA

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Screened
Output voltage	VDDA	Standby Mode (STBY), I_{LOAD} < 100 μA, VBAT > 0.90 V	1.7	1.8	1.9	V	✔
		Low ïPower Mode (LPM), I_{LOAD} = 100 μA, VBAT > 0.92 V	1.7	1.8	1.9	V	
							✔

VMIC

BANDGAP REFERENCED REGULATOR TEMPERATURE STABILITY

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Screened
Temperature Stability		Temperature range of ï5 to 50°C	ï0.5	ï	0.5	%	

NOTE: Temperature stability for VREG, VDDA (LPM and HPM), VMIC, VDDOD, VDDC (using the band gap as reference) and VDDM (using the band gap as reference):

PMU REFERENCED REGULATOR TEMPERATURE STABILITY

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Screened
Temperature Stability		Temperature range of ï5 to 50°C	ï2	ï	2	%	

NOTE: Temperature stability for VDDA (STBY), VDDC (using the PMU as reference) and VDDM (using the PMU as reference):

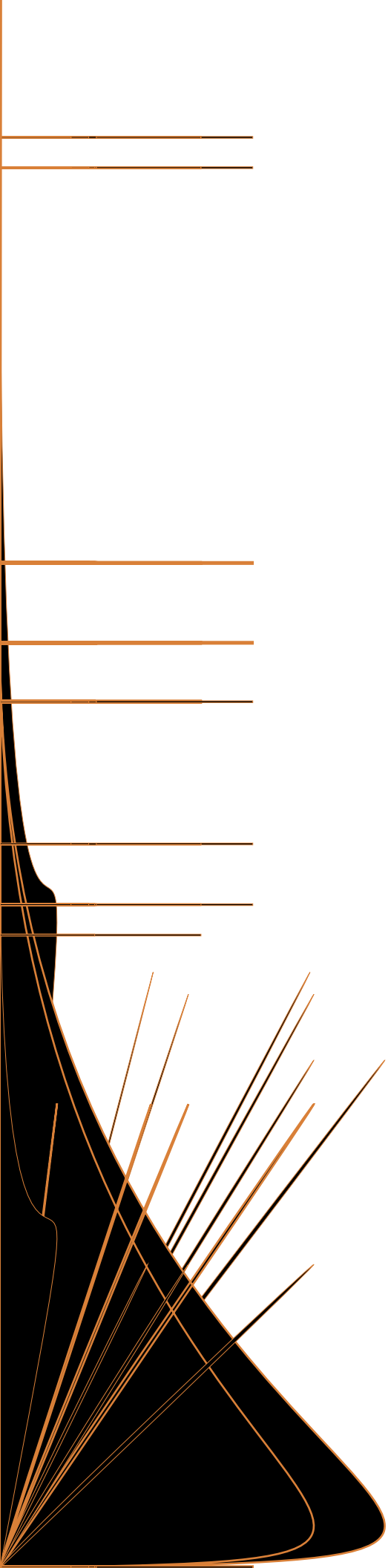
POWER ïON ïRESET

Description	Symbol	Conditions	Min	Typ	Max	Unit	Screened
VBAT startup voltage: High threshold voltage	Vth_{High}		0.68	0.77	0.86	V	✔
VBAT shutdown voltage: Low threshold voltage	Vth_{Low}		0.63	0.72	0.81	V	✔

NOTE: Typical time duration between application of VBAT and first NVM access: 77 ms

INPUT STAGE

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Screened
Nominal input referred noise 16 kHz SF, RMS	IN_{IRN}	A ïweighted 100 Hz ï8 kHz, 16 kHz SF, nominal current setting	ï	2	4	µVrms	
Nominal input referred noise 32 kHz SF, RMS		A ïweighted 100 Hz ï16 kHz, 32 kHz SF, maximum current setting	ï	3	10 (Note 11)	µVrms	✔
HiQ input referred noise 16 kHz SF, RMS		A ïweighted 100 Hz ï8 kHz, 16 kHz SF, maximum current setting	ï	1.5	3	µVrms	
HiQ input referred noise 48 kHz SF, RMS		A ïweighted 20 Hz ï20 kHz, 48 kHz SF, maximum current setting	ï	3	10 (Note 12)	µVrms	✔
Nominal dynamic range	IN_{DR}	A ïweighted 100 Hz ï8 kHz, nominal current setting	ï	109	ï	dB	
HiQ dynamic range		A ïweighted 100 Hz ï8 kHz, maximum current setting	ï	112	ï	dB	
Input range	IN_{RANGE}	At VDDA 1.8 V	0	ï	1.6	V	



IOs

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Screened
Strong pull ïup Impedance	IMP_{SUP}		0.8	1	1.2	kΩ	✔
Pad Input Delay	IN_{DELAY}	VDDO=1.8V	ï	ï	0.76	ns	
		VDDO=1.2V	ï	ï	1.23	ns	
Pad Output Delay	OUT_{DELAY}	VDDO=1.8V 1x drive strength, 1 pF load 2x drive strength, 2 pF load 4x drive strength, 4 pF load 8x drive strength, 8 pF load	ï	ï	1.24	ns	
		VDDO=1.2V 1x drive strength, 1pF load 2x drive strength, 2 pF load 4x drive strength, 4 pF load 8x drive strength, 8 pF load	ï	ï	1.74	ns	
Drive Strength	DRIVE	Configurable with 1x, 2x, 4x, 8x Nominal drive strength: 1 mA	1	ï	8	Multiple of the nominal drive strength	
Max Switching Frequency	$IOFR_{Max}$		Maximum SYS_CLK	ï	ï		
Glitch filter : additional rise delay	$DELAY_{RAISE}$		ï	ï	169	ns	
Glitch filter : additional fall delay	$DELAY_{FALL}$		ï	ï	245	ns	

NOTE: DC Characteristics of the digital pad at VDDO 1.08/1.8/1.98V

NOTE: The glitch filter cuts glitches with duration shorter than 50 ns

CURRENT CONTROLLED OSCILLATOR (CCO)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Screened
Recommended Working Frequency	SYS_CLK	For recommended VDDC and VDDM	2.56	ï	61.44	MHz	
Boot frequency	SYS_CLK		5	7.68	10	MHz	✔ ✔ ✔
Oscillator frequency trimming precision			ï	0.10	0.20	%	
Frequency stability in temperature		Temp: 0°C and 50°C. After calibration at room temperature (25°C)	ï1.5	ï	1.5	%	
		Temp: ï40°C and 85°C. After calibration at room temperature (25°C)	ï4	ï	4	%	
Period jitter (rms)		RMS, at 5.12 MHz, before multiplication	ï	ï	200	ps	
		RMS, at 5.12 MHz, after multiplied by 2 and divided by a multiple of 2	ï	ï	200	ps	
		RMS, at 5.12 MHz, after multiplied by 4 and divided by a multiple of 4	ï	ï	200	ps	
Output duty cycle		With multiplier setting 1x or 2x	45	ï	55	%	
		With multiplier setting 4x	40	ï	60	%	
Max frequency		Un ïmultiplied	ï	30	ï	MHz	

LOW DELAY PATH (using the low delay path of the Filter Engine)

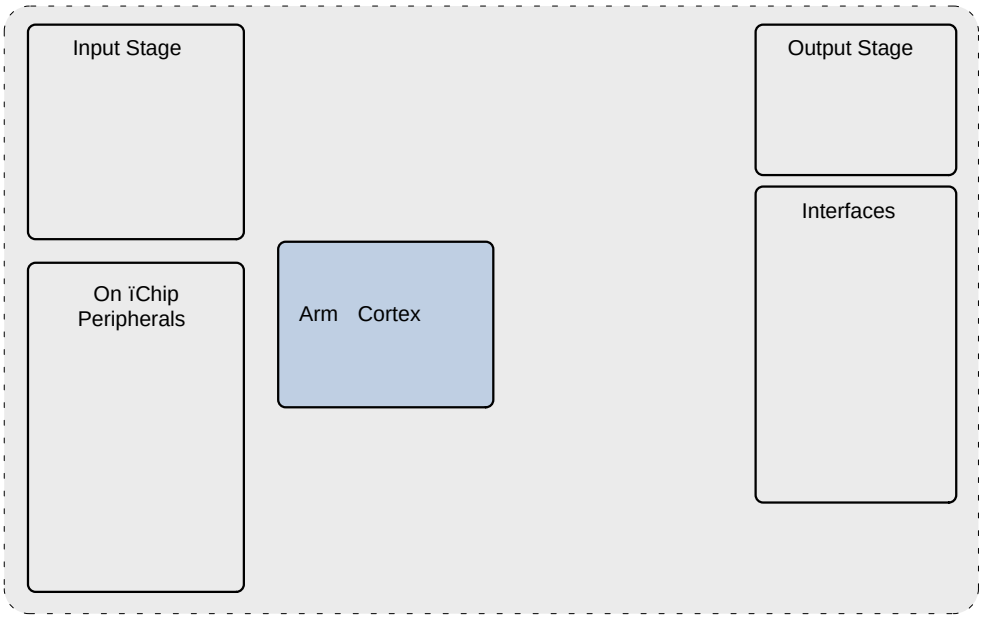
Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Screened
Analog to analog delay		Fs = 48 kHz FENG delay: one sample	ï	10.4	ï	s	

NVM (LE25S161)

Description	Symbol	Conditions	Min	Typ	Max	Unit	Sceened
Rewrite cylces, per Sector	cyc_{RW}	Per LE25161 datasheet	100’000			Cycles/ Sector	
Data Retention	t_{DRET}	Per LE25161 datasheet	20			year	
Program Mode Operating Current	I_{CCPPL}	Per LE25161 datasheet		5		mA	
Read Mode Operating Current	I_{CCR}	Per LE25161 datasheet		3.5		mA	

Ezairo 8310 System Diagram

Figure 1 isa simplified diagram of the hybrid system that shows the major internal functional blocks and possible external



ARCHITECTURE OVERVIEW

The Ezairo 8300 system is an asymmetric 6-core architecture, mixed-signal system-on-chip designed specifically for the audio processing needs of ultra-low power portable devices. It centers around 6 processing cores: the CFX Digital Signal Processor (DSP), the Arm Cortex-M3 Processor, the LPDSP32 Digital Signal Processor (DSP), the HEAR Configurable Accelerator, the Filter Engine and the Neural Network Accelerator.

CFX DSP Core

The CFX DSP is a user-programmable general-purpose DSP core that uses a 24-bit fixed-

- Feedback cancellation
- Noise reduction

To execute these and other algorithms efficiently, the HEAR excels at the following:

- Processing using a weighted overlap add (WOLA) filterbank
- Time domain filtering
- Subband filtering
- Attack/release filtering
- Vector addition/subtraction/multiplication
- Signal statistics (such as average, variance and correlation)

Filter Engine

The Filter Engine is a core that provides low delay path and basic filtering capabilities for the Ezairo 8300 system.

The Filter Engine can implement filters (either FIR or IIR) with a total of up to 320 coefficients. FIR filters are implemented using a direct form structure. IIR filters are implemented with a cascade of second order sections (biquads), each implemented as a direct form I filter.

The Filter Engine is programmable, but does not include direct debugging access. The CFX and the Arm Cortex−M3 Processor can monitor the Filter Engine state through control and configuration registers on the program memory bus.

LPDSP32 DSP

LPDSP32 is a 32−bit programmable, 32−bit DSP developed by onsemi. LPDSP32 is a high efficiency, dual Harvard DSP that supports both single (32−bit) and double precision (64−bit) arithmetic.

LPDSP32's dual MAC unit, load store architecture is specifically optimized to support audio processing tasks such as audio codecs that might be required for wireless audio communication tasks, Artificial Intelligence (AI) functions, and other advanced developments requiring the additional processing power that this core provides. The advanced architecture also provides:

- Two 72−bit ALUs capable of doing single and double precision arithmetic and logical operations
- Two 32−bit integer/fractional multipliers
- Four 64−bit accumulators with 8−bit overflow (extension bits)

The LPDSP32 relies on the CFX DSP or the Arm Cortex−M3 processor to initialize its memories and peripherals. Once initialized, the CFX DSP and/or the Arm Cortex−M3 processor control the LPDSP32 DSP's execution state.

Software development on the LPDSP32 is done in C.

Neural Network Accelerator (NNA)

The Neural Network Accelerator (NNA) is a hardware accelerator block that allows complex neural networks to run in an energy efficient manner. The accelerator can execute a single layer of a fully populated or sparsely populated neural network in a single task without any processor intervention. Layers with up to 1023 inputs and 1023 outputs are supported.

The NNA contains 16 multipliers, 16 accumulators, 16 input registers and 16 coefficient registers. It includes input and coefficient "fetchers" that, once configured, manage the data and coefficients memory access automatically. Support for coefficient compression/decompression and pruning is included and help minimize the amount of coefficient needed.

Other key components of the Ezairo 8300 are:

Memory systems: The memory systems provided by the Ezairo 8300 system are constructed using a number of memories (memory instances), memory buses, memory controllers and memory arbiters. These memories and other memory−mapped elements are addressable from the CFX DSP and the Arm Cortex−M3 processor through a set of memory spaces (also known as address spaces).

FIFO Controller: The Ezairo 8300 system's FIFO controller provides the ability to define up to 32 FIFO buffers.

Input/Output Controllers (IOC): The IOCs are responsible for handling input/output audio data. Samples can be routed along a number of different paths using the multiplexing options available in the Ezairo 8300 system.

Direct Memory Access (DMA) Controller: The direct memory access controller (DMA) module allows background transfers between components on the peripheral bus (referred to in this section as peripherals) and memories without any processor intervention. This allows the processors to be used for other computational needs while enabling high speed sustained transfers to and from the peripherals/memories. The DMA has 8 independent configurable channels.

Input Stage: The input stage of an Ezairo 8300 provides four audio input channels that supply signal data to the rest of the Ezairo 8300 system.

Output Stage: The output stage of Ezairo 8300 provides two audio output channels that post process signal data from the rest of the Ezairo 8300 system, and provide it to external receivers or speakers.

General Purpose Input/Output (GPIO) Pads: The Ezairo 8310 system offers 20 general purpose input/output (GPIO) pads that can be configured:

- To support the external interfaces, output clocks, and other I/Os
- As general−purpose I/Os (GPIO)
- Analog input/output function

The 20 GPIOs are split into four power domains. The voltages for these 4 power domains are given by:

- VDDO1 (GPIO5, GPIO7 to GPIO11) is supplied by VDDIF

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Ezairo 8310 HYBRID INTERFACE SPECIFICATIONS

A total of 49 pads are present on the Ezairo 8310 hybrid. These pads are the interfaces between the hybrid and the other components in the hearing aid. They are listed in the table below.

Ball Number	Hybrid Pad Name	Hybrid Pad Description
D10	VBATOD	Output driver power supply
E1	AI2	ADC analog input 2
E2	AI1	ADC analog input 1
E3	AI0	ADC analog input 0
E5	RCVR0P	Output Driver: Receiver Output 0 Positive
E6	RCVR0N	Output Driver: Receiver Output 0 Negative
E7	RCVR1P	Output Driver: Receiver Output 1 Positive
E8	RCVR1N	Output Driver: Receiver Output 1 Negative
E9	SCL	Debug port clock
E10	VSSOD	Output driver ground

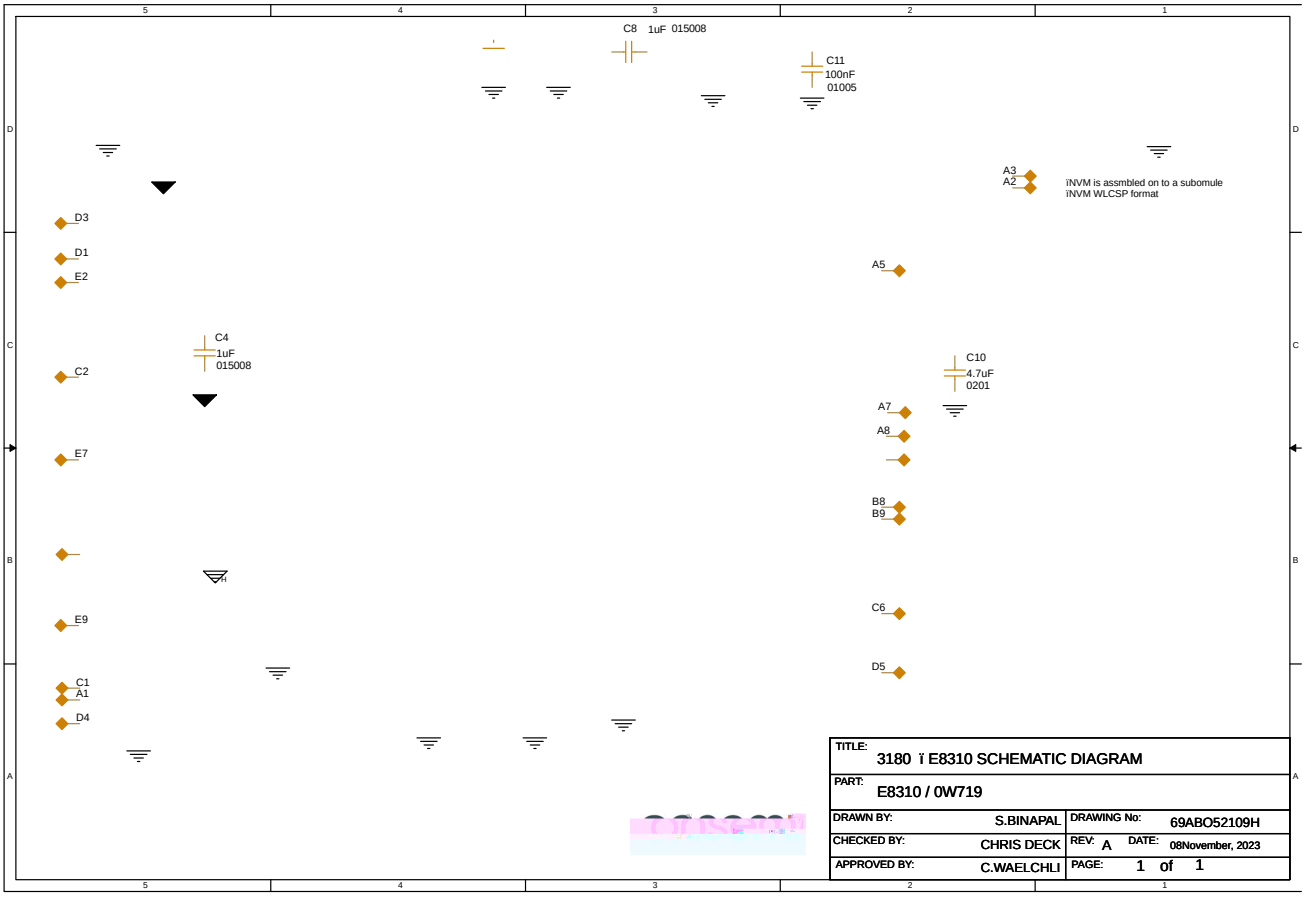

Figure 2. Ezairo 8310 Hybrid Schematics

Packaging and Manufacturing

- Ultra miniature form factor: suitable for all hearing aid styles including CIC, ITE, RITE, BTE, and mini BTE.
- Reflowable: the Ezairo 8310 hybrid is reflowable onto FR4 and other substrates.
- RoHS compliant: the Ezairo 8310 hybrid complies with the RoHS directive.

System Identification

System identification is used to identify different system components. This information can be retrieved using any of the supported communication box and protocol software provided by onsemi.

For the Ezairo 8300 chip, the key identifier components and values are as follows:

- Chip Family: 0x0A
- Chip Version: 0x01
- Chip Revision: 0x0101

The hybrid ID can be found in the manufacturing area of the NVM at address 0x00F1 to 0x00F2 (2 bytes => 16 bits).

- Hybrid ID: 0x00A0

Solder Information

The Ezairo 8310 hybrid is constructed with all RoHS compliant material with bump metallization of SAC305 (Sn96.5/Ag3.0/Cu0.5) solder and should therefore be reflowed accordingly. This hybrid device is Moisture Sensitive Class MSL3, 260°C and must be stored and handled accordingly. For soldering guidelines, please refer to the Soldering and Mounting Techniques Reference Manual (SOLDERRM/D). Hand soldering is not recommended for this part.

Electrostatic Discharge (ESD) Device

CAUTION: ESD sensitive device. Permanent damage may occur on devices subjected to high energy electrostatic discharges. Proper ESD precautions in handling, packaging and testing are recommended to avoid performance degradation or loss of functionality.

Development Tools

A full suite of comprehensive tools is available to assist software developers from the initial concept and technology assessment through to prototyping and product launch.

Application development and communication tools, as well as an Evaluation and Development Kit (EDK) facilitate the development of advanced algorithms on the Ezairo 8310 hybrid.

PACKAGE DIMENSIONS

SIP49 3.00x5.25
CASE 127FH
ISSUE A

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