M c 5.0 V, 100 A L D t L a R t a RESET a ENABLE

The CS8101 is a precision 5.0 V micropower voltage regulator with very low quiescent current (70 μA typ at 100 μA load). The 5.0 V output is accurate within ±2.0% and supplies 100 mA of load current with a typical dropout voltage of only 400 mV. Microprocessor control logic includes an $\overline{\text{ENABLE}}$ input and an active $\overline{\text{RESET}}$. This combination of low quiescent current, outstanding regulator performance and control logic makes the CS8101 ideal for any battery operated, microprocessor controlled equipment.

The active $\overline{\text{RESET}}$ circuit includes hysteresis, and operates correctly at an output voltage as low as 1.0 V. The $\overline{\text{RESET}}$ function is activated during the power up sequence or during normal operation if the output voltage drops outside the regulation limits by more than 200 mV typ. The logic level compatible $\overline{\text{ENABLE}}$ input allows the user to put the regulator into a shutdown mode where it draws only 20 μA typical of quiescent current.

The regulator is protected against reverse battery, short circuit, over voltage, and thermal overload conditions. The device can withstand load dump transients making it suitable for use in automotive environments.

The CS8101 is functionally e

September, 2008 − Rev. 19
Publication Order Number:
CS8101/D

CS8101

MAXIMUM RATINGS*

Rating	Value	Unit
Power Dissipation	Internally Limited	−
Peak Transient Voltage (46 V Load Dump @ V_{IN} = 14 V)	−15, 60	V
Operating DC Voltage	30	V
$\overline{\text{ENABLE}}$ (Up to V_{IN} with external resistor)	10	

ELECTRICAL CHARACTERISTICS (continued) (6.0 V ≤ V_{IN} ≤ 26 V; I_{OUT} = 1.0 mA; −40 ≤ T_A ≤ 125, −40°C ≤ T_J ≤ 150°C, unless otherwise noted.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
ENABLE Input ($\overline{ENABLE}$)					
Threshold HIGH LOW	 (V_{OUT} OFF) (V_{OUT} ON)	 − 0.6	 1.4 1.4	 2.0 −	 V V
Input Current	$V_{\overline{ENABLE}}$ = 2.4 V	−	30	100	μA
Reset Functions ($\overline{RESET}$)					
$\overline{RESET}$ Threshold HIGH (V_{RH}) LOW (V_{RL})	 V_{OUT} Increasing V_{OUT} Decreasing	 4.525 4.500	 4.75 4.70	 V_{OUT} − 0.05 V_{OUT} − 0.075	 V V
$\overline{RESET}$ Hysteresis	(HIGH − LOW)	25	50	100	mV
Reset Output Leakage $\overline{RESET}$ = HIGH	$V_{OUT} \geq V_{RH}$	−	−	25	μA
Output Voltage Low (V_{RLO}) Low (VR_{PEAK})	 1.0 V ≤ V_{OUT} ≤ V_{RL}, $R_{\overline{RESET}}$ = 10 k V_{OUT}, Power up, Power down, $R_{\overline{RESET}}$ = 10 k	 − −	 0.1 0.6	 0.4 1.0	 V V

PACKAGE LEAD DESCRIPTION

PACKAGE LEAD #			
SO−20 WB	**SOIC−8**	**LEAD SYMBOL**	**FUNCTION**
20	1	V_{OUT}	5.0 V, ±2.0%, 100 mA output.
−	2	V_{OUT}SENSE	Kelvin connection which allows remote sensing of output voltage for improved regulation. If remote sensing is not required, connect to V_{OUT}.
1	3	Active03 Rese(accurate88((V)Tj6.5 0 0 6.35203.628759.76 Tm-.0023 Tc0 Tw(OUT)Tj8 0 0 8 462.32 489.44 Tm0 Tc(	

TYPICAL PERFORMANCE CHARACTERISTICS

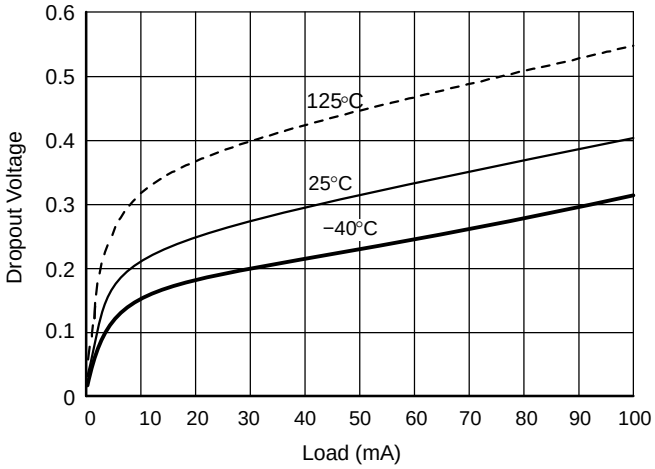


Figure 2. CS8101 Dropout Voltage vs. Load Over Temperature

CIRCUIT DESCRIPTION

VOLTAGE REFERENCE AND OUTPUT CIRCUITRY

Output Stage Protection

The output stage is protected against overvoltage, short circuit and thermal runaway conditions (Figure 3).

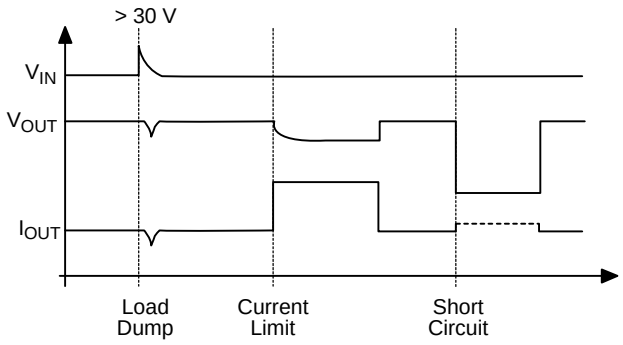


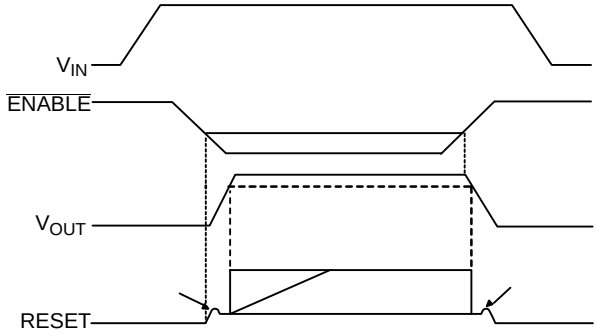
Figure 3. Typical Circuit Waveforms for Output Stage Protection

If the input voltage rises above 30 V (e.g. load dump), the output shuts down. This response protects the internal circuitry and enables the IC to survive unexpected voltage transients.

Should the junction temperature of the power device exceed 180°C (typ) the load current capability is reduced thereby preventing thermal overload. This thermal management function is an effective means to prevent die overheating since the load current is the principle heat source in the IC.

REGULATOR CONTROL FUNCTIONS

The CS8101 contains two microprocessor compatible control functions: $\overline{\text{ENABLE}}$ and $\overline{\text{RESET}}$ (Figure 4).



(1) = No Reset Delay Capacitor

Figure 4. Circuit Waveform

The $\overline{\text{RESET}}$ output is an open collector NPN transistor, controlled by a low voltage detection circuit. The circuit is functionally independent of the rest of the IC thereby guaranteeing that the $\overline{\text{RESET}}$ signal is valid for V_{OUT} as low as 1.0 V.

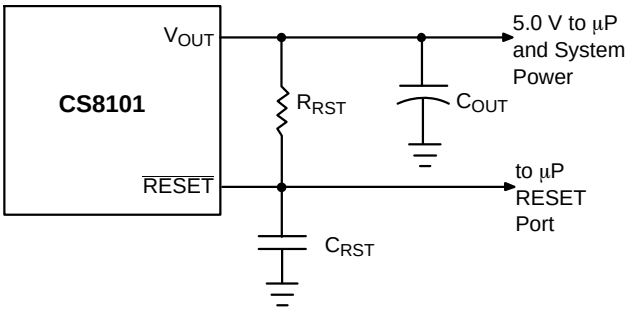


Figure 5. RC Network for $\overline{\text{RESET}}$ Delay

An external RC network on the lead (Figure 5) provides a sufficiently long delay for most microprocessor based applications. RC values can be chosen using the following formula:

$$R_{TOT}C_{RST} = \left[\frac{-t_{Delay}}{\ln\left(\frac{V_T - V_{OUT}}{V_{RST} - V_{OUT}}\right)}\right]$$

where:

R_{RST} = $\overline{\text{RESET}}$ Delay resistor
R_{IN} = μP port impedance
R_{TOT} = R_{RST} in parallel with R_{IN}
C_{RST} = $\overline{\text{RESET}}$ Delay capacitor
t_{Delay} = desired delay time
V_{RST} = V_{SAT} of $\overline{\text{RESET}}$ lead (0.7 V @ turn − ON)
V_T = $\overline{\text{RESET}}$ threshold.

The circuit depicted in Figure 6 lets the microprocessor control its power source, the CS8101 regulator. An I/O port on the μP and the SWITCH port are used to drive the base of Q1. When Q1 is driven into saturation, the voltage on the $\overline{\text{ENABLE}}$ lead falls below its lower threshold. The regulator's output is enabled. When the drive current is removed, the voltage on the $\overline{\text{ENABLE}}$ lead rises, the output is switched off and the IC moves into Sleep mode where it draws 50 μA (max).

By coupling these two controls with the $\overline{\text{ENABLE}}$ lead, the system has added flexibility. Once the system is running,

APPLICATION NOTES

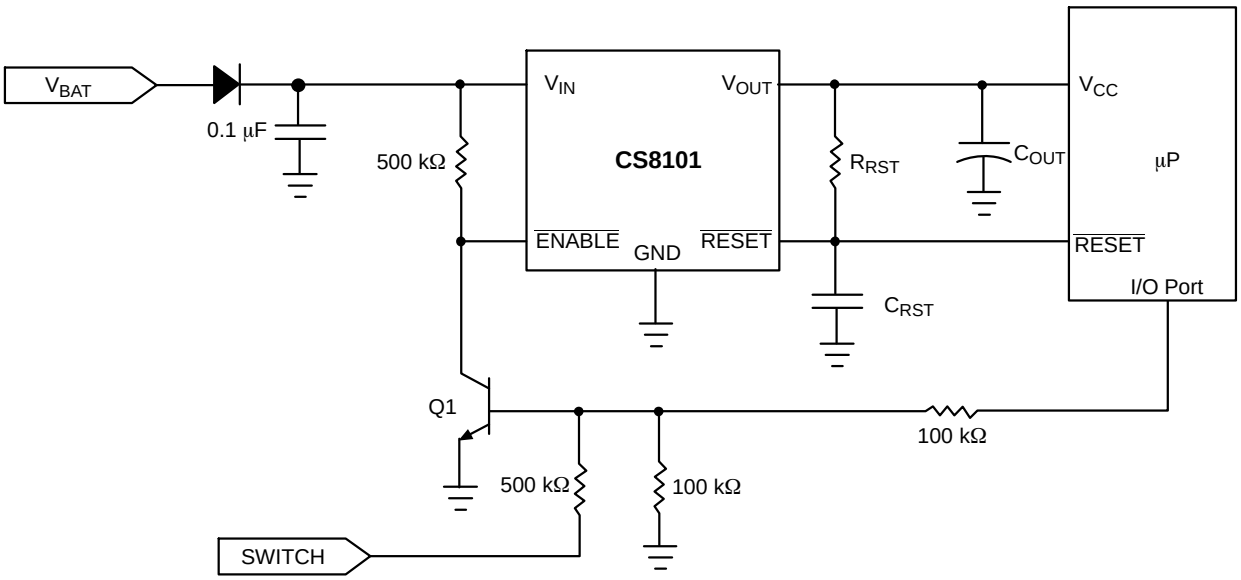


Figure 6. Microprocessor Control of CS8101 Using External Switching Transistor Q1

The $\overline{ENABLE}$ pin of the CS8101 can be tied to the battery voltage provided a series resistor is used as shown in Figure 7. The maximum allowed voltage on the $\overline{ENABLE}$ pin without the resistor is 10 V. Direct voltages greater than 10 V applied to the pin without the series resistor may damage the device. The system designer should note the turn−on threshold (typ 1.4 V) is on the $\overline{ENABLE}$ pin. The threshold will be higher on the other side of $R_{\overline{ENABLE}}$.

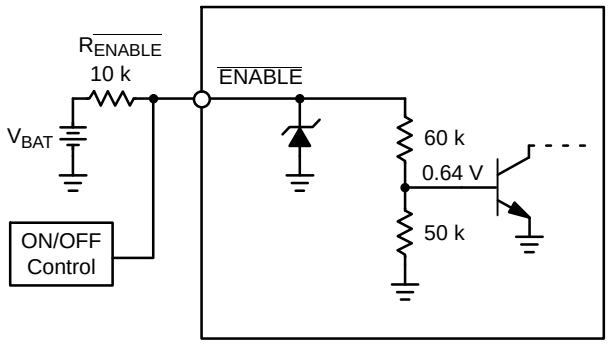
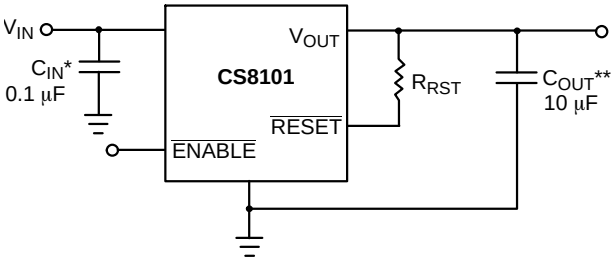


Figure 7. Using the $\overline{ENABLE}$ pin with V_{BAT}

STABILITY CONSIDERATIONS

The output or compensation capacitor helps determine three main characteristics of a linear regulator: start−up delay, load transient response and loop stability.



*C_{IN} required if regulator is located far from the power supply filter.

*C_{OUT} required for stability. Capacitor must operate at minimum temperature expected.

Figure 8. Test and Application Circuit Showing Output Compensation

The capacitor value and type should be based on cost, availability, size and temperature constraints. A tantalum or aluminum electrolytic capacitor is best, since a film or ceramic capacitor with almost zero ESR can cause instability. The aluminum electrolytic capacitor is the least expensive solution, but, if the circuit operates at low temperatures (−25°C to −40°C), both the value and ESR of the capacitor will vary considerably. The capacitor manufacturers data sheet usually provides this information.

The value for the output capacitor C_{OUT} shown in Figure 8 should work for most applications, however it is not necessarily the optimized solution.

To determine an acceptable value for C_{OUT} for a particular application, start with a tantalum capacitor of the recommended value and work towards a less expensive alternative part.

Step 1: Place the completed circuit with a tantalum

DEVICE ORDERING INFORMATION*

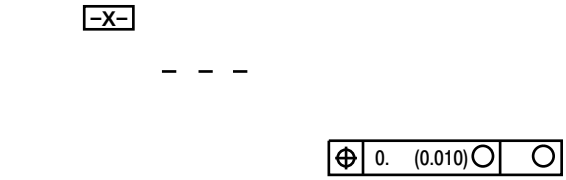
Device	Package	Shipping†
CS8101YD8G	SOIC−8 (Pb−Free)	98 Units/Rail
CS8101YDR8G	SOIC−8 (Pb−Free)	2500/Tape & Reel
CS8101YDWF20G	SO−20 WB (Pb−Free)	38 Units/Tube
CS8101YDWFR20G	SO−20 WB (Pb−Free)	1000/Tape & Reel

*Contact your local sales representative for D^2PAK package option.

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MARKING DIAGRAMS

SO−20 WB



C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0	8	0	8
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

0. (0.010) 1 0 1 1 0 0 1 . 0 0 0 0 . 1 1 0 1 1 . 1 0 . 0 0 0 1 . 1 1 0 0 1 1 0 ( ) 0 1 . 1 1 0 0 1 1 . 1 1 . 1 0 0 . 0 0 0 . 1 1 . 1 0 0 . 0 0 0 1 1 . 1 0 0 0 1 0 0 0 0 .)

SOIC−20 WB
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