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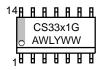
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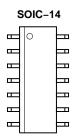
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MARKING DIAGRAM

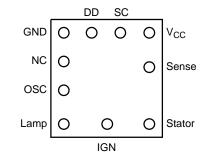




**PIN CONNECTIONS** 



#### Flip Chip, Bump Side Up



 $V_{CC}$ 

IGN

Sense

LAMP

 $V_{SUP}$ 

Figure 1. Block Diagram

**ELECTRICAL CHARACTERISTICS** (-40°C <  $T_A$  < 125°C, -40°C <  $T_J$  < 150°C, 9.0 V ≤  $V_{CC}$  ≤

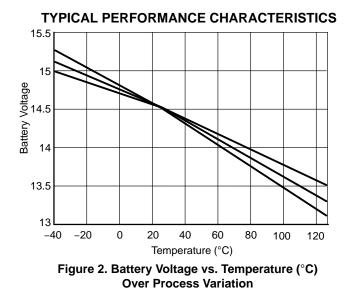
#### PACKAGE PIN DESCRIPTION

PACKAGE PIN #							
SOIC-14	Flip Chip	PIN SYMBOL	FUNCTION				
1	1	Driver	Output driver for external power switch-Darlington				
2	2	GND	Ground				
3, 6, 7, 9, 13	3	NC	No Connection				
4	4	OSC	Timing capacitor for oscillator				
5	5	Lamp	Base driver for lamp driver indicates no stator signal or overvoltage condition				
8	6	IGN	Switched ignition powerup				
10	7	Stator	Stator signal input for stator timer (CS3351 also powerup)				
11	8	Sense	Battery sense voltage regulator comparator input and protection				
12	9	V <sub>CC</sub>	Supply for IC				
14	10	SC	Short circuit sensing				

#### **ORDERING INFORMATION**

Device	Package	Shipping <sup>†</sup>
CS3341YD14	SOIC-14	55 Units/Rail
CS3341YD14G	SOIC-14 (Pb-Free)	55 Units/Rail
CS3341YDR14	SOIC-14	2500 Tape & Reel
CS3341YDR14G	SOIC-14 (Pb-Free)	2500 Tape & Reel
CS3351YD14	SOIC-14	55 Units/Rail
CS3351YD14G	SOIC-14 (Pb-Free)	55 Units/Rail
CS3351YDR14	SOIC-14	2500 Tape & Reel
CS3351YDR14G	SOIC-14 (Pb-Free)	2500 Tape & Reel
CS387H	Flip Chip	Contact Sales

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



#### **REGULATION WAVEFORMS**

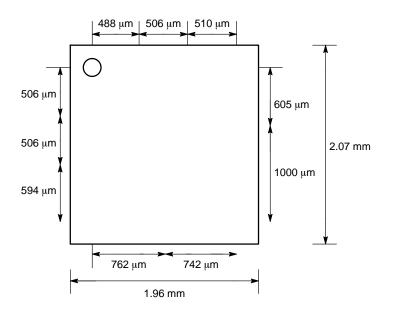
The CS3341/3351/387 utilizes proportion control to maintain regulation. Waveforms depicting operation are shown in Figures 4, 5 and 6, where  $V_{BAT/N}$  is the divided down voltage present on the Sense pin using R1 and R2 (Figure 7). A sawtooth waveform is generated internally. The amplitude of this waveform is listed in the electric parameter section as proportion control. The oscillator voltage is summed with  $V_{BAT/N}$ , and compared with the internal voltage regulator ( $V_{REG}$ ) in the regulation

comparator which controls the field through the output "Device Driver."

Figure 4 shows typical steady state operation. A 50% duty cycle is maintained.

Figure 5 shows the effect of a drop in voltage on ( $V_{BAT/N}$  +  $V_{OSC}$ ). Notice the duty cycle increase to the field drive.

Figure 6 shows the effect of an increase in voltage (above the regulation voltage) on  $(V_{BAT/N} \ensuremath{\mathsf{AT/N}}$ 

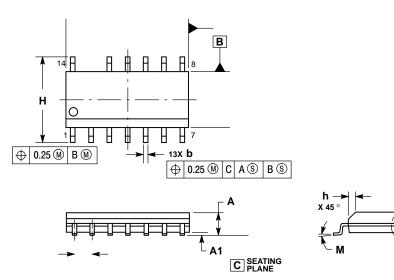




SOIC 14 NB CASE 751A-03 ISSUE L

DATE 03 FEB 2016





- NOTES:
  1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
  2. CONTROLLING DIMENSION: MILLIMETERS.
  3. DIMENSION & DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
  4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
  5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

SIDE.

#### GENERIC **MARKING DIAGRAM\***

14	A	Ħ	A	Ħ	A	A	<u> </u>
		xx	XX	хх	хх	XG	
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XXXXX	= Specific Device Code
A	= Assembly Location
WL	= Wafer Lot
Y	= Year
WW	= Work Week
G	= Pb-Free Package

#### **STYLES ON PAGE 2**

DATE 03 FEB 2016

STYLE 7: PIN 1. ANODE/CATHODE 2. COMMON ANODE 3. COMMON CATHODE 4. ANODE/CATHODE 5. ANODE/CATHODE

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