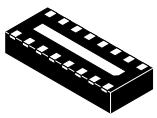
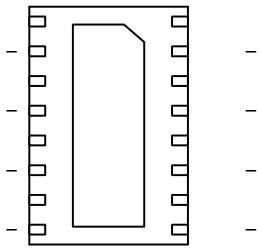
http://onsemi.com



WDFN16
DE SUFFIX
CASE 511BG

PINOUT DIAGRAM



ORDERING INFORMATION

Features

- ESD Protection for 4 Pairs of Differential Channels
- ESD Protection to:
  - IEC61000 4 2 Level 4 (ESD) at ±8 kV Contact Discharge
  - IEC61000 4 4 (EFT) 40 A (5/50 ns)
  - IEC61000 4 5 (Lighting) 3.5 A (8/20 μs)
- Pass through Impedance Matched Clamp Architecture
- Flow through Routing for High speed Signal Integrity
- Minimal Line Capacitance Change with Temperature and Voltage
- 100 Ω Matched Impedance for Each Paired Differential Channel
- Each I/O Pin can Withstand Over 1000 ESD Strikes*
- RoHS Compliant (lead free), Small Footprint 4.0 mm x 1.7 mm WDFN 16 Package

Applications

- DVI, DisplayPort, and HDMI Ports in Notebooks, Set Top Boxes, Digital TVs, and LCD Displays
- General Purpose High speed Data Line ESD Protection

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January, 2014

corresponding ports in removable storage, digital camcorders, DVD RW drives and other applications where extremely low loading

Figure 1. Block Diagram

ESD Protection Architecture

Conceptually, an ESD protection device performs the following actions upon an ESD strike discharge into a protected ASIC (see Figure 2):

1. When an ESD potential is applied to the system under test (contact or air discharge), Kirchoff's Current Law (KCL) dictates that the Electrical Overstress (EOS) currents will immediately divide throughout the circuit, based on the dynamic impedance of each path.

2. Ideally, the classic shunt ESD clamp will switch within 1 ns to a low impedance path and return

The Architecture Advantages

PIN DESCRIPTIONS

Pin	Name	Description
	–	
	–	
	–	
	–	
	–	
	–	
	–	
	–	

Specifications

Table 1. ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Units
	–	°
	–	°

Table 2. ELECTRICAL OPERATING CHARACTERISTICS

° °

Symbol	Parameter	Conditions	Min	Typ	Max	Units
			–			
		°		±	±	µ
	–	°	±			
	– –					
		– –				
		Ω °				
		°				
	– –	µ				
				–		
		°				Ω
		µ				
		Ω				Ω
						Ω
Δ	– –					

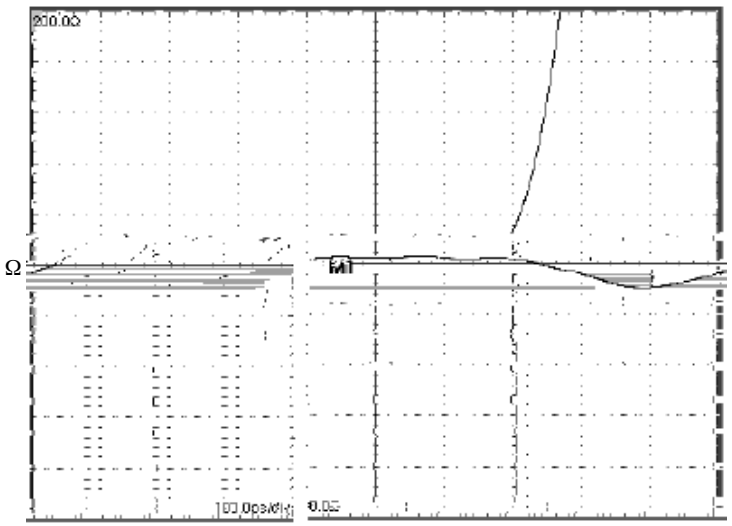


Figure 8. Typical Channel TDR Measured Across Out_x and In_x Per Each Differential Channels Pair (Typical 200 ps Incident Rise Time)

Application Information

CM1235 Application and Guidelines

As a general rule, the CM1235 ESD protection array should be located as close as possible to the point of entry of expected electrostatic discharges with minimum PCB trace lengths to the ground planes and between the signal input and the ESD device to minimize stray series inductance.

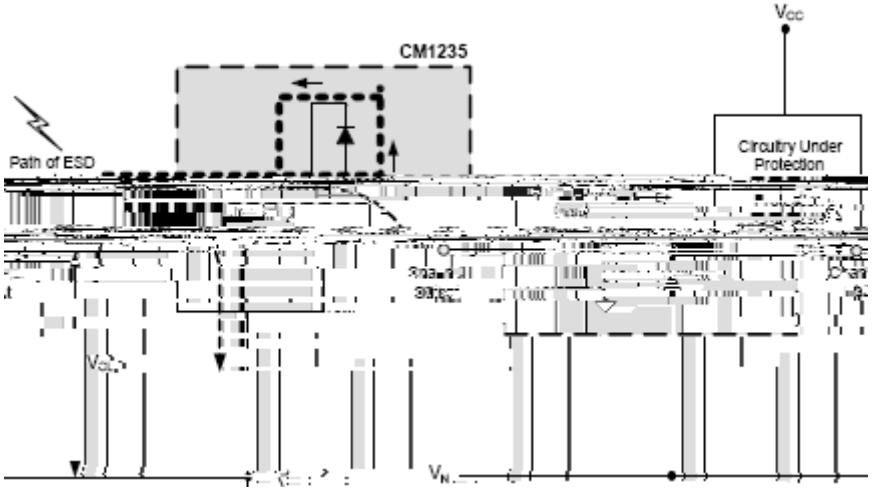


Figure 9. Application of Positive ESD Pulse Between Input Channel and Ground

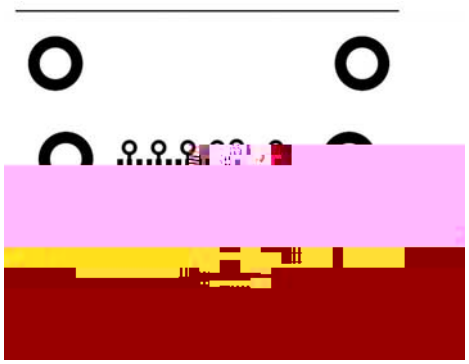


Figure 10. Typical PCB Layout

Additional Information

See also ON Semiconductor Application Note “Design Considerations for ESD Protection,” in the Applications section at www.onsemi.com.

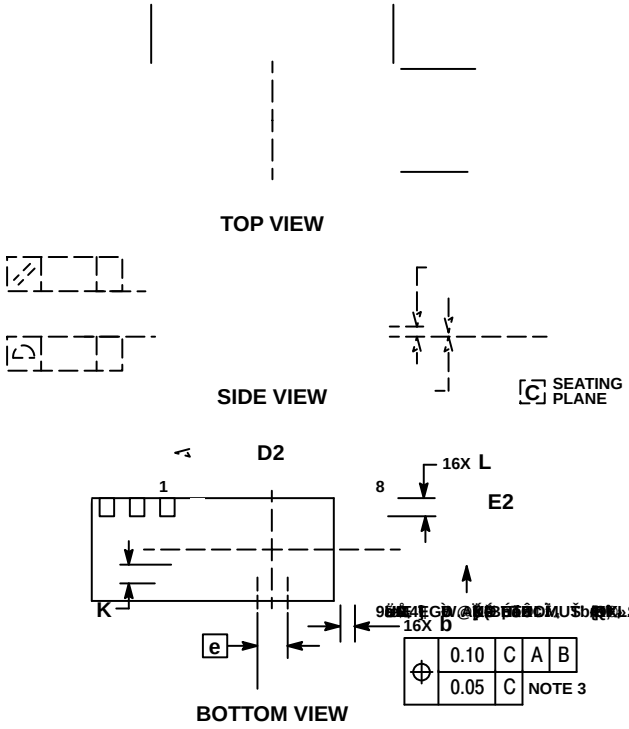
Ordering Information

PART NUMBERING INFORMATION

Pin	Package	Ordering Part Number (Lead Free Finish)	Part Marking
	–	–	

TAPE AND REEL SPECIFICATIONS

Part Number	Package Size (mm)



WDFN16, 4X1.7, 0.5P