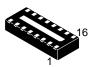


http://onsemi.com



WDFN16 **DE SUFFIX** CASE 511BG

Features

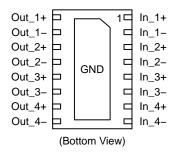
- ESD Protection for 4 Pairs of Differential Channels
- ESD Protection to:
 - IEC61000 4 2 Level 4 (ESD) at ±8 kV Contact Discharge
 - IEC61000 4 4 (EFT) 40 A (5/50 ns)
 - IEC61000 4 5 (Lighting) 3.5 A (8/20 μs)
- Pass through Impedance Matched Clamp Architecture
- Flow through Routing for High speed Signal Integrity
- Minimal Line Capacitance Change with Temperature and Voltage
- 100 Ω Matched Impedance for Each Paired Differential Channel
- Each I/O Pin can Withstand Over 1000 ESD Strikes*
- RoHS Compliant (lead free), Small Footprint 4.0 mm x 1.7 mm WDFN 16 Package

Applications

- DVI, DisplayPort, and HDMI Ports in Notebooks, Set Top Boxes, Digital TVs, and LCD Displays
- General Purpose High speed Data Line ESD Protection

*Standard test condition is IEC61000-4-2 level 4 test circuit with each pin subjected to ±8 kV contact discharge for 1000 pulses. Discharges are timed at 1 second intervals and all 1000 strikes are completed in one continuous test run. The part is then subjected to standard production test to verify that all of the tested parameters are within spec after the 1000 strikes.

PINOUT DIAGRAM



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.

Figure 1. Block Diagram

ESD Protection Architecture

Conceptually, an ESD protection device performs the following actions upon an ESD strike discharge into a protected ASIC (see Figure 2):

- 1. When an ESD potential is applied to the system under test (contact or air discharge), Kirchoff's Current Law (KCL) dictates that the Electrical Overstress (EOS) currents will immediately divide throughout the circuit, based on the dynamic impedance of each path.
- 2. Ideally, the classic shunt ESD clamp will switch within 1 ns to a low impedance path and return

The Architecture Advantages			

PIN DESCRIPTIONS

Pin	Name	Description
1	ln_1+	Bidirectional Clamp to ASIC (inside system)
2	In_1-	Bidirectional Clamp to ASIC (inside system)
3	In_2+	Bidirectional Clamp to ASIC (inside system)
4	In_2-	Bidirectional Clamp to ASIC (inside system)
5	In_3+	Bidirectional Clamp to ASIC (inside system)
6	In_3-	Bidirectional Clamp to ASIC (inside system)
7	In_4+	Bidirectional Clamp to ASIC (inside system)
8	In_4-	Bidirectional Clamp to ASIC (inside system)
9	Out_4-	Bidirectional Clamp to Connector (outside system)
10	Out_4+	Bidirectional Clamp to Connector (outside system)
11	Out_3-	Bidirectional Clamp to Connector (outside system)
12	Out_3+	Bidirectional Clamp to Connector (outside system)
13	Out_2-	Bidirectional Clamp to Connector (outside system)
14	Out_2+	Bidirectional Clamp to Connector (outside system)
15	Out_1-	Bidirectional Clamp to Connector (outside system)
16	Out_1+	Bidirectional Clamp to Connector (outside system)
PAD	GND	Ground return to shield

Specifications

Table 1. ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Units
Operating Temperature Range	-40 to +85	°C
Storage Temperature Range	-65 to +150	°C
Breakdown Voltage (Positive)	6	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 2. ELECTRICAL OPERATING CHARACTERISTICS (All parameters specified at $T_A = -40^{\circ}\text{C}$ to +85°C unless otherwise noted.)

Symbol	Parameter	Conditions	Min	Тур	Max	Units
V _{IN}	I/O Voltage Relative to GND		-0.5		5.5	V
I _{IN}	Continuous Current through signal pins (IN to OUT) 1000 Hr			100		mA
IF	Channel Leakage Current	T _A = 25°C; V _{IN} = 5 V		±0.1	±1.0	μΑ
V _{ESD} ESD Protection – Peak Discharge Voltage at any channel input, in system: Contact discharge per IEC 61000–4–2 Standard		T _A = 25°C	±8			kV
I _{RES} Residual ESD Peak Current on RDUP (Resistance of Device Under Protection)		IEC 61000–4–2 8 kV; RDUP = 5 Ω , T _A = 25°C; See Figure 7		3.0		А
V _{CL}	Channel Clamp Voltage (Channel clamp voltage per IEC 61000–4–5 Standard) Positive Transients Negative Transients	$I_{PP} = 1 \text{ A}, T_A = 25^{\circ}\text{C},$ $t_P = 8/20 \mu\text{S}$		+9.2 -1.6		V
R _{DYN}	Dynamic Resistance Positive Transients Negative Transients	$I_{PP} = 1 \text{ A}, T_A = 25^{\circ}\text{C},$ $t_P = 8/20 \mu\text{S}$		0.6 0.5		Ω
Z _{TDR}	Differential Impedance	TDR excursion from 100 Ω characteristic impedance transmission line; TR = 200 ps; (Note 1)	87		103	Ω
Zo	Differential Channels pair characteristic impedance	T _R = 200 ps; (Note 1)		100		Ω
ΔΖο	Channel-to-Channel Impedance Match Continuoom 100	•	•	1	•	•

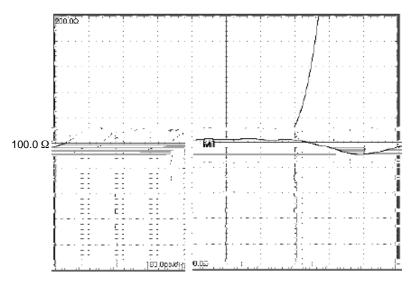


Figure 8. Typical Channel TDR Measured Across Out_x and In_x Per Each Differential Channels Pair (Typical 200 ps Incident Rise Time)

Application Information

CM1235 Application and Guidelines

As a general rule, the CM1235 ESD protection array should be located as close as possible to the point of entry of expected electrostatic discharges with minimum PCB trace lengths to the ground planes and between the signal input and the ESD device to minimize stray series inductance.

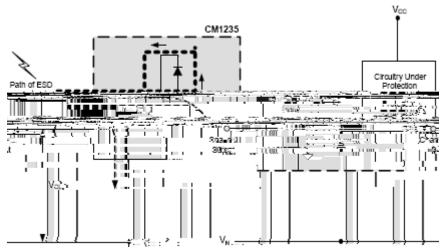


Figure 9. Application of Positive ESD Pulse Between Input Channel and Ground

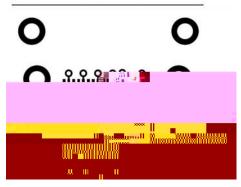


Figure 10. Typical PCB Layout

Additional Information

See also ON Semiconductor Application Note "Design Considerations for ESD Protection," in the Applications section at www.onsemi.com.

Ordering Information

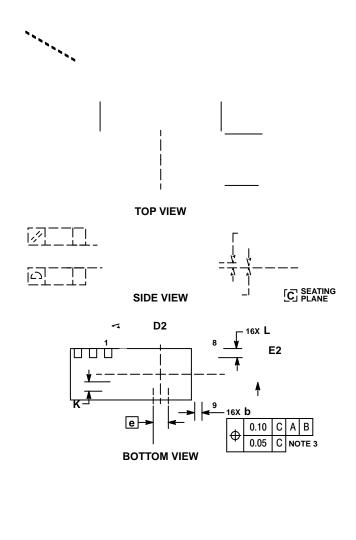
PART NUMBERING INFORMATION

Pin	Package	Ordering Part Number (Lead Free Finish)	Part Marking
16	WDFN-16	CM1235-08DE	CM1235

NOTE: Parts are shipped in Tape & Reel form unless otherwise specified.

TAPE AND REEL SPECIFICATIONS †

Part Number Package Size (mm)



DOCHMENT, NUMBER:	98AON48938E	Electronic versions are uncontrolled except when
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