Table 1. PIN DESCRIPTION

TSSOP	TQFN	Pin Name	Function
1	22	A0	Address Input 0
2	23	A1	Address Input 1
3	24	A2	Address Input 2
4−11	1−8	LED0 − LED7	LED Driver Output 0 to 7, I/O Port 0 to 7
12	9	V_{SS}	Ground
13−20	10−17	LED8 − LED15	LED Driver Output 8 to 15, I/O Port 8 to 15
21	18	$\overline{\text{RESET}}$	Reset Input
22	19	SCL	Serial Clock
23	20	SDA	Serial Data
24	21	V_{CC}	Power Supply

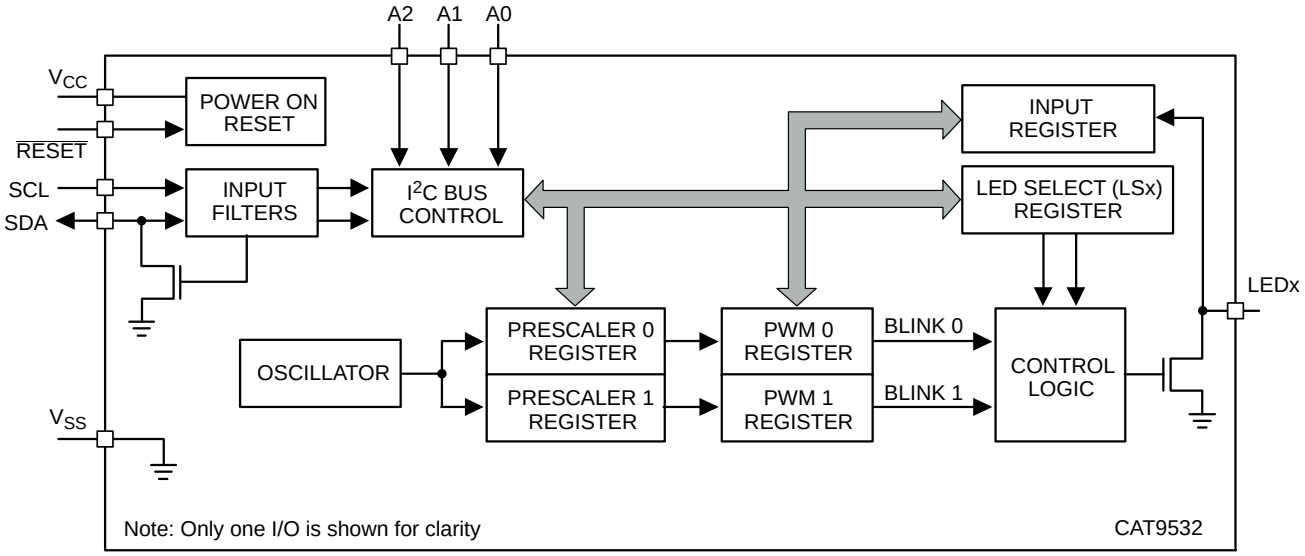


Figure 3. Block Diagram

Table 2. ABSOLUTE MAXIMUM RATINGS

Parameters	Ratings	Units
V_{CC} with Respect to Ground	−0.3 to +7.0	V
Voltage on Any Pin with Respect to Ground	−0.3 to +5.5	V
DC Current on I/Os	±25	mA
Supply Current	400	mA
Package Power Dissipation Capability (T_A = 25°C)	1.0	

Table 3. D.C. OPERATING CHARACTERISTICS (V_{CC} = 2.3 to 5.5 V, V_{SS} = 0 V; T_A = −40°C to +85°C, unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SUPPLIES						
V_{CC}	Supply Voltage		2.3	−	5.5	V

Table 4. A.C. CHARACTERISTICS (V_{CC} = 2.3 V to 5.5 V, T_A = −40°C to +85°C, unless otherwise specified) (Note 5)

Symbol	Parameter	Standard I^2C		Fast I^2C		Units
		Min	Max	Min	Max	
F_{SCL}						

Pin Description

SCL: Serial Clock

The serial clock input clocks all data transferred into or out of the device. The SCL line requires a pull−up resistor if it is driven by an open drain output.

SDA: Serial Data/Address

The bidirectional serial data/address pin is used to transfer all data into and out of the device. The SDA pin is an open drain output and can be wire−ORed with other open drain or open collector outputs. A pull−up resistor must be connected from SDA line to V_{CC}.

LED0 to LED15: LED Driver Outputs / General Purpose I/Os

The pins are open drain outputs used to drive directly LEDs. Any of these pins can be programmed to drive the LED ON, OFF, Blink Rate1 or Blink Rate2. When not used for controlling the LEDs, these pins may be used as general purpose parallel input/output.

$\overline{\text{RESET}}$: External Reset Input

Active low Reset input is used to initialize the CAT9532 internal registers and the I^2C state machine. The internal registers are held in their default state while Reset input is active. An external pull−up resistor of maximum 25 kΩ is required when this pin is not actively driven.

Functional Description

The CAT9532 is a 16−bit I/O bus expander that provides a programmable LED dimmer, controlled through an I^2C compatible serial interface.

The CAT9532 supports the I^2C Bus data transmission protocol. This Inter−Integrated Circuit Bus protocol defines any device that sends data to the bus to be a transmitter and any device receiving data to be a receiver. The transfer is controlled by the Master device which generates the serial clock and all START and STOP conditions for bus access. The CAT9532 operates as a Slave device. Both the Master device and Slave device can operate as either transmitter or receiver, but the Master device controls which mode is activated.

I^2C Bus Protocol

The features of the I^2C bus protocol are defined as follows:

1. Data transfer may be initiated only when the bus is not busy.
2. During a data transfer, the data line must remain stable whenever the clock line is high. Any changes in the data line while the clock line is high will be interpreted as a START or STOP condition (Figure 5).

START and STOP Conditions

The START Condition precedes all commands to the device, and is defined as a HIGH to LOW transition of SDA when SCL is HIGH. The CAT9532 monitors the SDA and SCL lines and will not respond until this condition is met.

A LOW to HIGH transition of SDA when SCL is HIGH determines the STOP condition. All operations must end with a STOP condition.

Device Addressing

After the bus Master sends a START condition, a slave address byte is required to enable the CAT9532 for a read or write operation. The four most significant bits of the slave address are fixed as binary 1100 (Figure 6). The CAT9532

Acknowledge

After a successful data transfer, each receiving device is required to generate an acknowledge. The acknowledging device pulls down the SDA line during the ninth clock cycle, signaling that it received the 8 bits of data. The SDA line remains stable LOW during the HIGH period of the acknowledge related clock pulse (Figure 7).

The CAT9532 responds with an acknowledge after receiving a START condition and its slave address. If the device has been selected along with a write operation, it responds with an acknowledge after receiving each 8− bit byte.

When the CAT9532 begins a READ mode it transmits 8 bits of data, releases the SDA line, and monitors the line for an acknowledge. Once it receives this acknowledge, the CAT9532 will continue to transmit data. If no acknowledge is sent by the Master, the device terminates data transmission and waits for a STOP condition.

The Input Register 0 and Input Register 1 reflect the incoming logic levels of the I/O pins, regardless of whether the pin is defined as an input or an output. These registers are read only ports. Writes to the input registers will be acknowledged but will have no effect.

Table 7. INPUT REGISTER 0 AND INPUT REGISTER 1

INPUT0								
	LED 7	**LED 6**	**LED 5**	**LED 4**	**LED 3**	**LED 2**	**LED 1**	**LED 0**
bit	7	6	5	4	3	2	1	0
default	X	X	X	X	X	X	X	X
INPUT1								
	LED 15	**LED 14**	**LED 13**	**LED 12**	**LED 11**	**LED 10**	**LED 9**	**LED 8**
bit	7	6	5	4	3	2	1	0
default	X	X	X	X	X	X	X	X

The Frequency Prescaler 0 and Frequency Prescaler 1 registers (PSC0, PSC1) are used to program the period of the pulse width modulated signals BLINK0 and BLINK1 respectively:

$T\_BLINK0 = (PSC0 + 1) / 152;$
$T\_BLINK1 = (PSC1 + 1) / 152$

Table 8. FREQUENCY PRESCALER 0 AND FREQUENCY PRESCALER 1 REGISTERS

PSC0								
bit	7	6	5	4	3	2	1	0
default	0	0	0	0	0	0	0	0
PSC1								
bit	7	6	5	4	3	2	1	0
default	0	0	0	0	0	0	0	0

The PWM Register 0 and PWM Register 1 (PWM0, PWM1) are used to program the duty cycle of BLINK0 and BLINK1 respectively:

$Duty\ Cycle\_BLINK0 = PWM0 / 256;$
$Duty\ Cycle\_BLINK1 = PWM1 / 256$

After writing to the PWM0/1 register an 8−bit internal

Write Operations

Data is transmitted to the CAT9532 registers using the write sequence shown in Figure 9.

If the AI bit from the command byte is set to “1”, the CAT9532 internal registers can be written sequentially. After sending data to one register, the next data byte will be sent to the next register sequentially addressed.

Read Operations

The CAT9532 registers are read according to the timing diagrams shown in Figure 10 and Figure 12. Data from the register, defined by the command byte, will be sent serially on the SDA line.

After the first byte is read, additional data bytes may be read when the auto−increment flag, AI, is set. The additional data byte will reflect the data read from the next register sequentially addressed by the (B3 B2 B1 B0) bits of the command byte.

When reading Input Port Registers (Figure 12), data is clocked into the register on the failing edge of the acknowledge clock pulse. The transfer is stopped when the master will not acknowledge the data byte received and issue

Application Information

Programming Example

The following programming sequence is an example how to set:

- LED0 to LED3: ON
- LED4 to LED7: Dimming at 30% brightness; Blink 1: 152 Hz, duty cycle 30%
- LED8 to LED11: Blink at 2 Hz with 50% duty cycle (Blink 2)
- LED12 to LED15: OFF

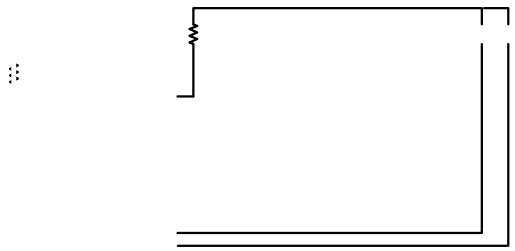


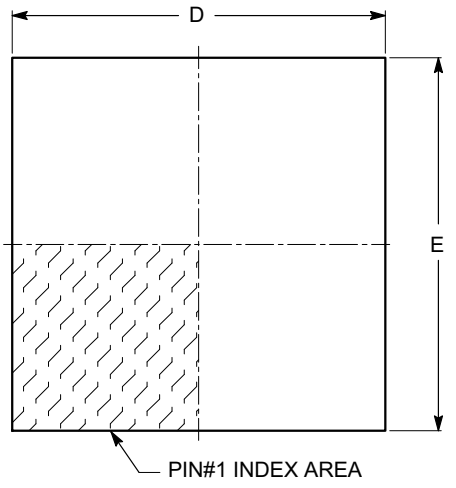
Figure 14. Typical Applicationf66 Tc 0T 1 1 0-Tw (f66 Tc 0T 1 1 0-Tw (f66.6 lSQq1 0 0 1 1622.791501.5847 554.91 m709

Ordering Information (Notes 9 to 13)

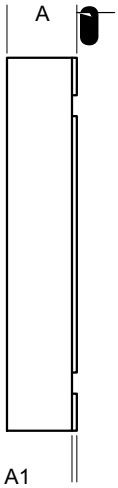
9. All packages are RoHS−compliant (Lead−free, Halogen−free).

TQFN24, 4x4
CASE 510AG−01
ISSUE B

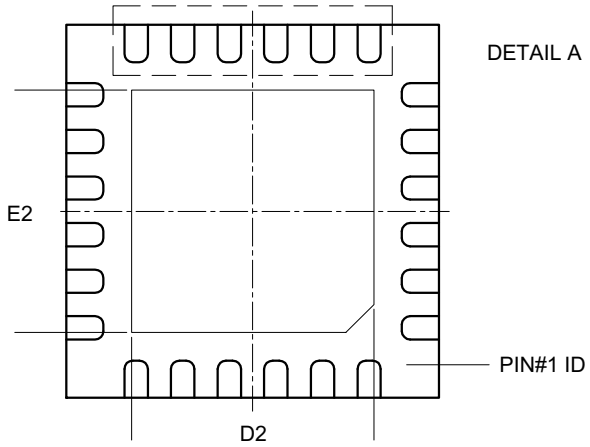
DATE 04 DEC 2009



TOP VIEW



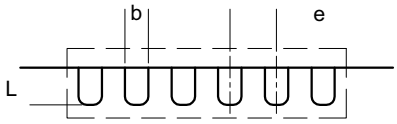
SIDE VIEW



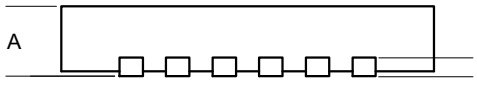
BOTTOM VIEW

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00		0.05
A3		0.20 REF	
b	0.20	0.25	0.30
D		4.00 BSC	
D2	2.70	2.80	2.90
E		4.00 BSC	
E2	2.70	2.80	2.90
e		0.50 BSC	
L	0.30		0.50

Notes:
(1) All dimensions are in millimeters.
(2) Conforms to JEDEC MO-220.



DETAIL A



FRONT VIEW

A3

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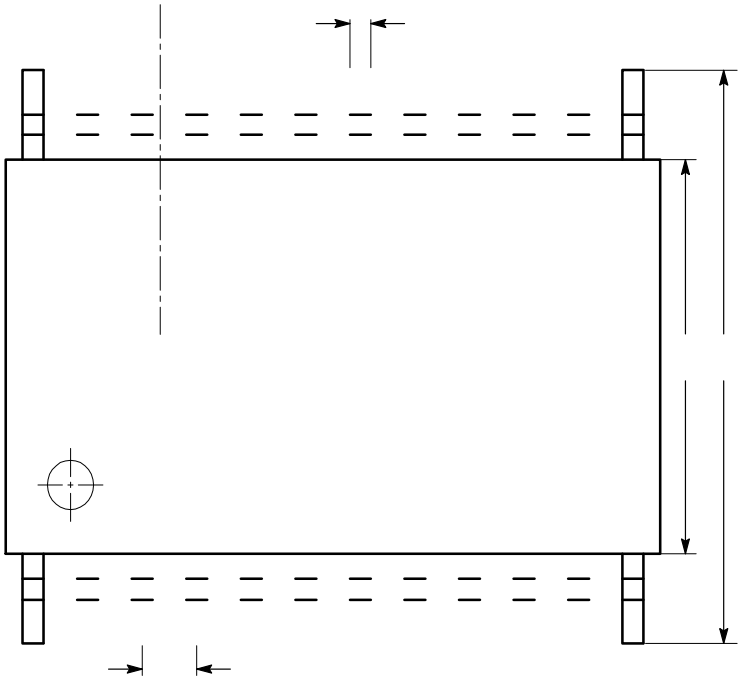
TSSOP24, 4.4x7.8
CASE 948AR−01
ISSUE A

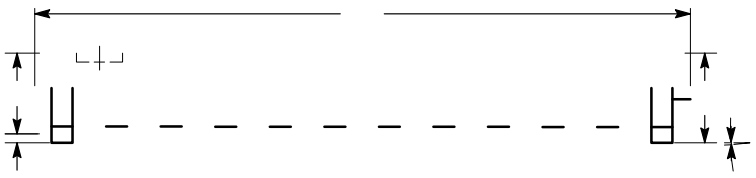
DATE 17 MAR 20090101

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

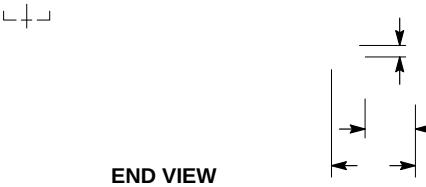


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			1.20
A1	0.05		0.15
A2	0.80		1.05
b	0.19		0.30
c	0.09		0.20
D	7.70	7.80	7.90
E	6.25	6.40	6.55
E1	4.30	4.40	4.50
e		0.65 BSC	
L	0.50	0.60	0.70
L1		1.00 REF	



SIDE VIEW



END VIEW

Notes: