CAT874

Sma Ph ne Ba e S i ch C n lle

Description

CAT874 is a switch controller designed to start/shut−off smart phones with the push button input or by phone microcontroller unit.

CAT874 monitors two inputs and outputs an active high output after PWR_ON input has been active (logic low) for a factory preset minimum time. Releasing input from its active state before the minimum timeout period resets the internal timer and must return to being active before the timer will restart with a fresh count down. The output remains high until the next PWR_ON high−

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Publication Order Number:
CAT874/D

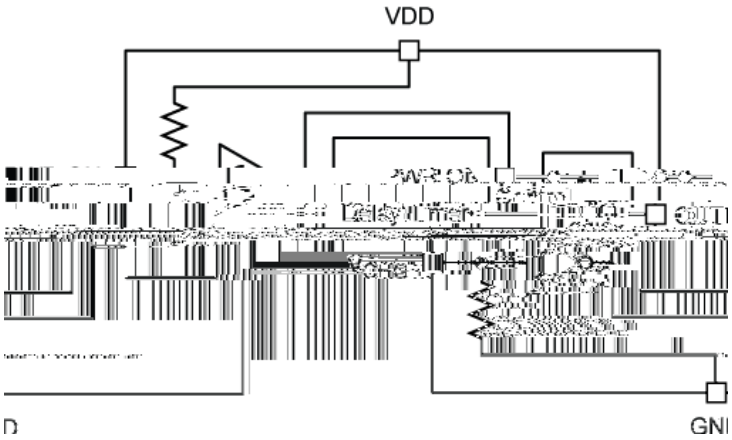


Figure 2. Functional Block Diagram

Table 1. PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Description
1		

Table 4. ELECTRICAL OPERATING CHARACTERISTICS
(V_{DD} = 1.8 V to 5.5 V. For typical values T_A = 25°C, for min/max values T_A = −40°C to +85°C unless otherwise noted.)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
POWER						
V_{DD} Supply Voltage		V_{DD}	1.8		5.5	V
Quiescent Supply Current	PWR_ON = VDD, V_{CHG} = 0 V	I_{DD}		100		

TIMING WAVEFORMS

H

H

Figure 3. Timing Waveforms

SYSTEM DESCRIPTION AND APPLICATIONS INFORMATION

General

CAT874 is designed for the manual switching of microprocessors and microcontrollers. To prevent accidental resets, CAT874 requires PWR_ON input be held low for a prescribed period before an Active high output is issued to the system processor.

PWR_ON and V_{CHG} Inputs

PWR_ON and V_{CHG} are Schmitt trigger CMOS inputs. PWR_ON must go low and stay low for a predetermined period (t_{LOW_DELAY}) to generate an Active high on the output.

V_{CHG} is a standard CMOS input with internal pull down resistor 200 kΩ to keep the input low when charger is not plugged in and PWR_ON is also a CMOS input with an internal 200 kΩ pull−up resistor, thus PWR_ON can be left floating.

When PWR_ON goes low, an internal timing cycle is initiated. If it goes high before the countdown timer has concluded its cycle, the timer will reset and will restart from the beginning when PWR_ON returns to being low.

Output (OUT)

CAT874 provides an active−high push pull output. This output will sink up to 3 mA.

Delay Timer Testing:

A user test mode is provided to reduce the system test time after the CAT874 is mounted on the board. Instead of waiting t_{LOW_DELAY} for the output to go active.

The user brings PWR_ON low, and sends seven positive edges on the V_{CHG} pin in a window of time t_{ST}. After a delay t_D, the device output will change state from low to high, and will return to the low state only when there is a high−to−low transition on PWR_ON.

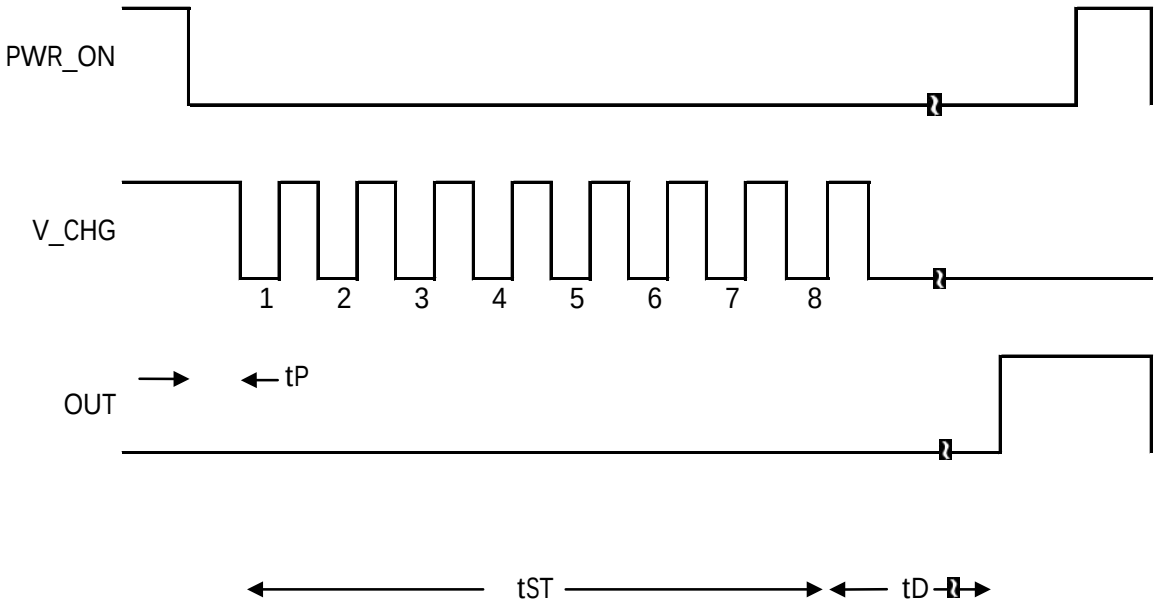
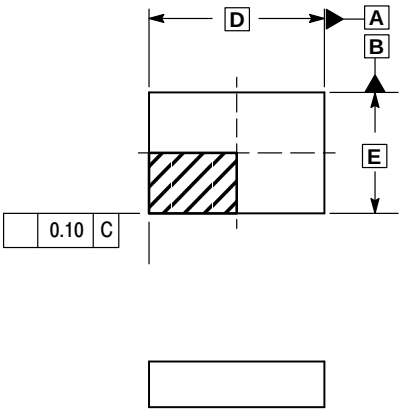


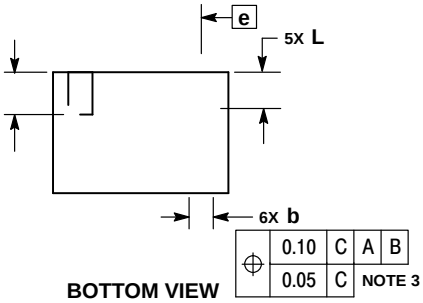
Figure 4. TOC Mode

ULLGA6, 1.45x1.0, 0.5P
CASE 613AF−01
ISSUE A

DATE 06 FEB 2008

SCALE 8:1





BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.
4. A MAXIMUM OF 0.05 PULL BACK OF THE PLATED TERMINAL FROM THE EDGE OF THE PACKAGE IS ALLOWED.

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