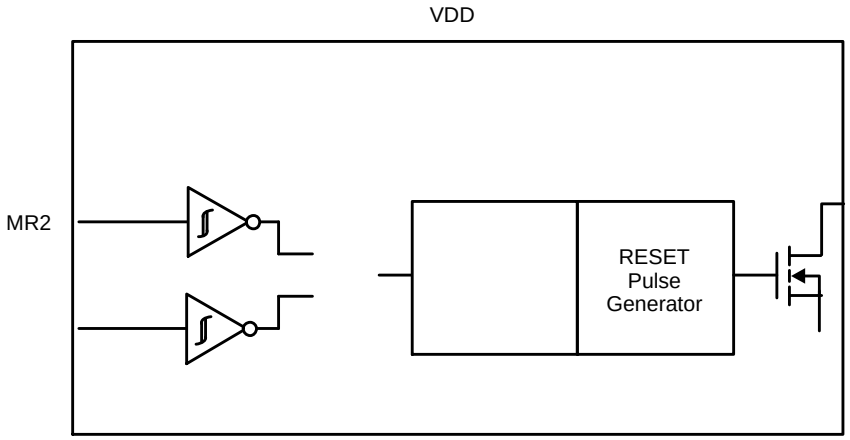
CAT871, CAT872

D a l · R G a

CAT871, CAT872 are dual input reset generators designed to restart microprocessor and microcontroller based systems when the watchdog timer or other resetting mechanisms have become disabled or failed.

CAT871, CAT872 monitor two inputs and output an active low reset pulse after both inputs have been active (logic low) for a factory preset minimum time. The reset pulse width is 2.2 ms for CAT871 and 70 ms for CAT872. Releasing either input from its active state before the minimum timeout period resets the internal timer and both inputs must return to being active before the timer will restart with a fresh count

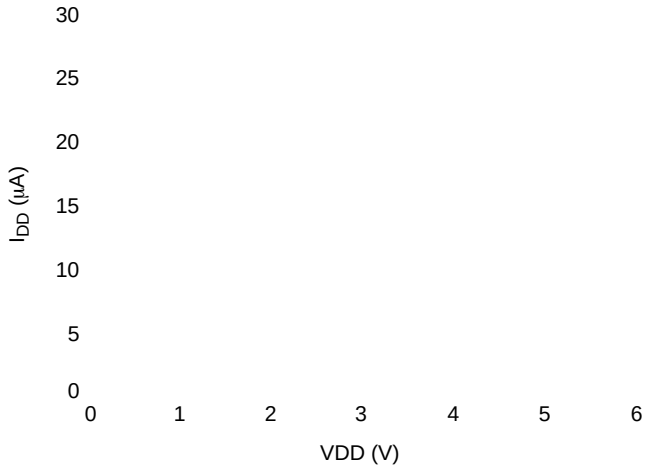
Publication Order Number:

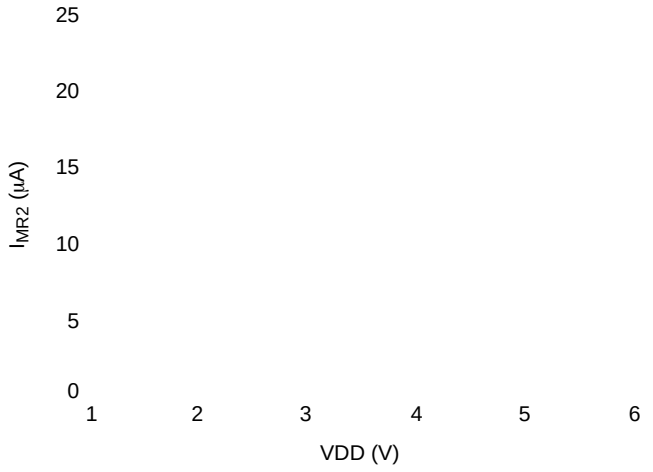

VDD
MR2
RESET
Pulse
Generator

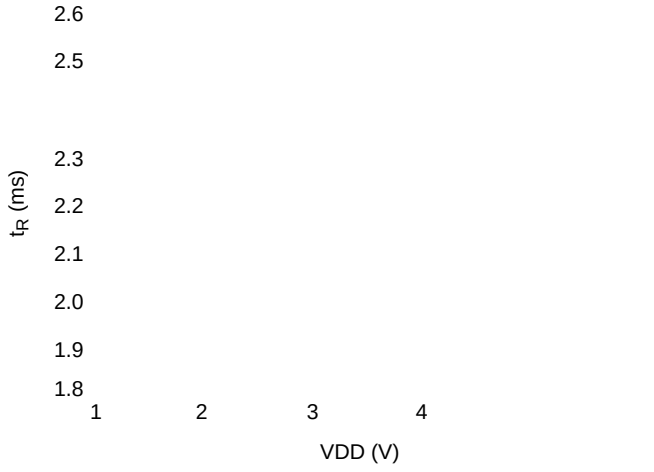
Input Voltage; VDD	V_{DD}	1.65	5.5	V
Input Voltage; MR1, MR2	V_{IN}	0	V_{DD}	V
Output Current; $\overline{\text{RESET}}$	I_{OUT}	0	3	mA
Ambient Temperature	T_A	−40	85	°C

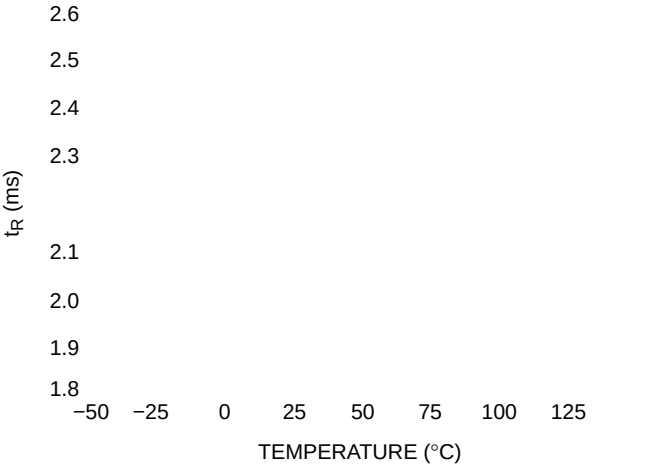
(V_{DD} = 1.65 V to 5.5 V. For typical values T_A = 25°C, for min/max values T_A = −40°C to +85°C unless otherwise noted.)

V_{DD} Supply Voltage		V_{DD}	1.65		5.5	V
Quiescent Supply Current	MR1 = MR2 = V_{DD}.	I_{DD}		10	1000	nA
Operating Supply Current	MR1 = MR2 = 0 V Measured during setup period. Measurement includes current through internal 200 kΩ pull−up resistor on MR2				50	μA
Input Voltage; HIGH	MR1, MR2	V_{IH}	0.7 x V_{DD}			V
Input Voltage; LOW	MR1, MR2	V_{IL}			0.25xV_{DD}	V
Hysteresis		V_{HYS}	−	250		mV
Input Current	MR1 = 0 V; V_{DD} = 5 V (no internal pull−up)	I_{PU}		50	300	nA
Input Current	MR2 = 0 V; V_{DD} = 5 V (internal 200 kΩ pull−up resistor)	I_{PU}		25		μA


30
25
20
15
10
5
0
I_{DD} (µA)
0
1
2
3
4
5
6
VDD (V)


25
20
15
10
5
0
I_{MR2} (µA)
1
2
3
4
5
6
VDD (V)


2.6
2.5
2.3
2.2
2.1
2.0
1.9
1.8
t_R (ms)
1
2
3
4
VDD (V)


2.6
2.5
2.4
2.3
2.1
2.0
1.9
1.8
t_R (ms)
−50
−25
0
25
50
75
100
125
TEMPERATURE (°C)

CAT871, CAT872 are designed for the manual resetting of microprocessors and microcontrollers when normal resetting mechanisms have failed. To prevent accidental resets, CAT871, CAT872 require both manual reset inputs be held low for a prescribed period before a reset pulse is issued to the system processor.

MR1 and MR2 are Schmitt trigger CMOS inputs. Both inputs must go low and stay low for a predetermined period (t_{LOW_DELAY}) to generate a single reset pulse on the output. MR1 and MR2 operate independently and may be brought low at any time and in any order. The last input to reach 0 V starts the delay timer.

MR1 is a standard CMOS input and MR2 is also a CMOS input with an internal 200 kΩ pull−up resistor, thus MR2 can be left floating whereas MR1 must be biased by a pull−up resistor, powered switch or some other means external to the IC. (Consult factory for other input biasing options)

When both MR1 and MR2 go low, an internal timing cycle is initiated. If any input goes high before the countdown

When both MR1 and MR2 inputs are kept low, a single reset pulse is generated after the delay t_{LOW_DELAY}. Even with both MR1 and MR2 maintained low continuously after that time, no second reset pulse will be generated. The delay timer restarts if either MR1 or MR2 (or both) input transitions from high to low, as shown in the timing diagram in Figure 13.

The reset generator can be used in a system where the supply VDD is different than the MR1, MR2 input logic. Figure 14 shows an application schematic where the

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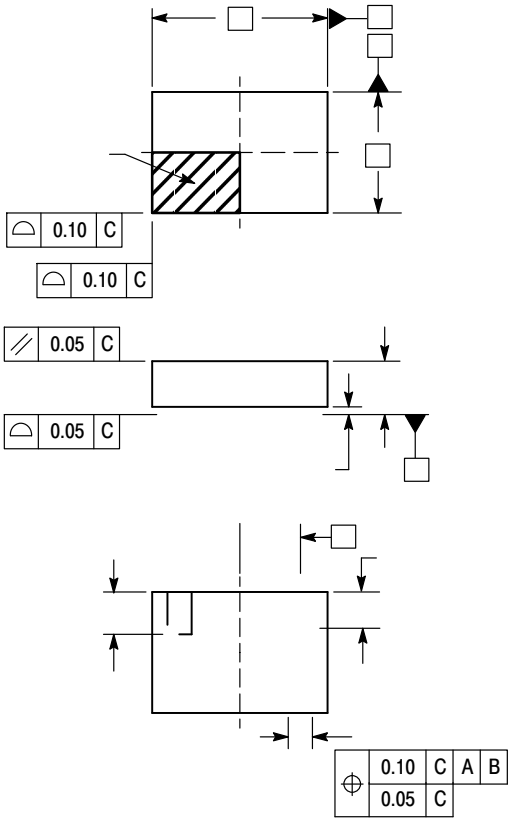

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.
4. A MAXIMUM OF 0.05 PULL BACK OF THE PLATED TERMINAL FROM THE EDGE OF THE PACKAGE IS ALLOWED.

ULLGA6, 1.45x1.0, 0.5P
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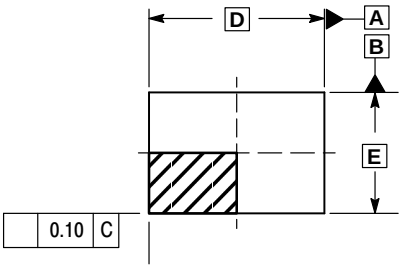
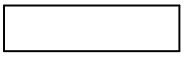
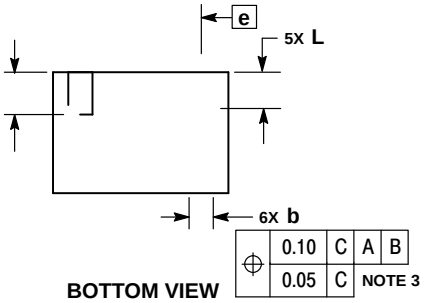
DATE 06 FEB 2008

SCALE 8:1







BOTTOM VIEW

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