June, 2024 − Rev. 10

Figure 1. Block Diagram

Table 3. ELECTRICAL OPERATING CHARACTERISTICS
(DC Characteristics: V_{CC} = 3.0 V to 5.5 V for M version; V_{CC} = 2.0 V to 3.6 V for the R/S/T/U/Y/Z version, −40°C ≤ T_A ≤ +85°C unless otherwise noted. Typical Values at T_A = 25°C and V_{CC} = 5 V for M version; V_{CC} = 3.3 V for the T/S versions; V_{CC} = 3.0 V for the R version; and V_{CC} = 2.5 V for the U/Y/Z versions.) (Note 1)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{CC}	Supply Current	CAT824 (M Version)		6	17	μA
		CAT823 (R/S/T/Y/Z Versions) CAT824 (M/U Versions)		4	12	
V_{RST}	Reset Threshold	CAT82_M at −40°C ≤ T_A ≤ +85°C	4.25	4.38	4.50	V
		CAT82_T at −40°C ≤ T_A ≤ +85°C	3.00	3.08	3.15	
		CAT82_S at −40°C ≤ T_A ≤ +85°C	2.85	2.93	3.00	
		CAT82_R at −40°C ≤ T_A ≤ +85°C	2.55	2.63	2.70	
		CAT82_Z at −40°C ≤ T_A ≤ +85°C	2.25	2.32	2.38	
		CAT82_Y at −40°C ≤ T_A ≤ +85°C	2.13	2.19	2.25	
		CAT824U at −40°C ≤ T_A ≤ +85°C	1.95	2.00	2.05	
	Reset Threshold Tempco			40		ppm/°C
	Reset Threshold Hysteresis	CAT82_M		10		mV
		CAT82_R/S/T/Y/Z, CAT824U		5		
t_{RD}	V_{CC} to Reset Delay (Note 2)	V_{CC} = V_{TH} to (V_{TH} − 100 mV)		20		μs
t_{RP}	Reset Active Timeout Period		140	200	400	ms
V_{OH}	$\overline{\text{RESET}}$ Output High Voltage	CAT82_M, V_{CC} = $V_{RST\ max}$, I_{SOURCE} = −120 μA	V_{CC} − 1.5 V			V
		CAT82_T/S/R/Z/Y, CAT824U, V_{CC} = $V_{RST\ max}$, I_{SOURCE} = −30 μA	0.8 x V_{CC}			
V_{OL}	$\overline{\text{RESET}}$ Output Low Voltage	CAT82_M, V_{CC} = $V_{RST\ min}$, I_{SINK} = 3.2 mA			0.4	V
		CAT82_T/S/R/Z/Y, CAT824U, V_{CC} = $V_{RST\ min}$, I_{SINK} = 1.2 mA			0.3	
		T_A = 0°C to +70°C, V_{CC} = 1 V, V_{CC} falling, I_{SINK} = 50 μA			0.3	
		T_A = T_{MIN} to T_{MAX}, V_{CC} = 1.2 V, V_{CC} falling, I_{SINK} = 100 μA			0.3	
I_{SOURCE}	$\overline{\text{RESET}}$ Output Short−Circuit Current	CAT82_M, Reset = 0 V, V_{CC} = 5.5 V			1.5	mA
		CAT82_M, Reset = 0 V, V_{CC} = 3.6 V			0.8	
V_{OH}	Reset Output Voltage	V_{CC} > 1.8 V, I_{SOURCE} = −150 μA	0.8 x V_{CC}			V
V_{OL}		CAT824M, V_{CC} = $V_{RST\ max}$, I_{SINK} = 3.2 mA			0.4	
		CAT824M/U, V_{CC} = $V_{RST\ max}$, I_{SINK} = 1.2 mA			0.3	
WATCHDOG INPUT (CAT823 & CAT824)						
t_{WD}	Watchdog Timeout Period		1.12	1.60	3.20	s
t_{WDI}	WDI Pulse Width	V_{IL} = 0.4 V, V_{IH} = 0.8 x V_{CC}	50			

Table 3. ELECTRICAL OPERATING CHARACTERISTICS (continued)
(DC Characteristics: V_{CC} = 3.0 V to 5.5 V for M version; V_{CC} = 2.0 V to 3.6 V for the R/S/T/U/Y/Z version, −40°C ≤ T_A ≤ +85°C unless otherwise noted. Typical Values at T_A = 25°C and V_{CC} = 5 V for M version; V_{CC} = 3.3 V for the T/S versions; V_{CC} = 3.0 V for the R version; and V_{CC} = 2.5 V for the U/Y/Z versions.) (Note 1)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
MANUAL RESET INPUT (CAT823)						
V_{IL}	$\overline{MR}$ Input Voltage				0.3 x V_{CC}	V
V_{IH}			0.7 x V_{CC}			
t_{PB}	$\overline{MR}$ Pulse Width		1			μs
t_{PDLY}	$\overline{MR}$ low to Reset Delay				5	μs
	$\overline{MR}$ Noise Immunity	Pulse Width with No Reset		100		ns
	$\overline{MR}$ Pullup Resistance (internal)		35	52	75	kΩ

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. Over−temperature limits are guaranteed by design and not production tested.
2. The RESET short−circuit current is the maximum pull−up current when reset is driven low by a bidirectional output.
3. WDI is internally serviced within the watchdog period if WDI is left open.
4. The WDI input current is specified as an average input current when the WDI input is driven high or low. The WDI input if connected to a three−stated output device can be disabled in the tristate mode as long as the leakage current is less than 10 μA and a maximum capacitance of less than 200 pF. To clock the WDI input in the active mode the drive device must be able to source or sink at least 200 μA when active.

TYPICAL ELECTRICAL OPERATING CHARACTERISTICS

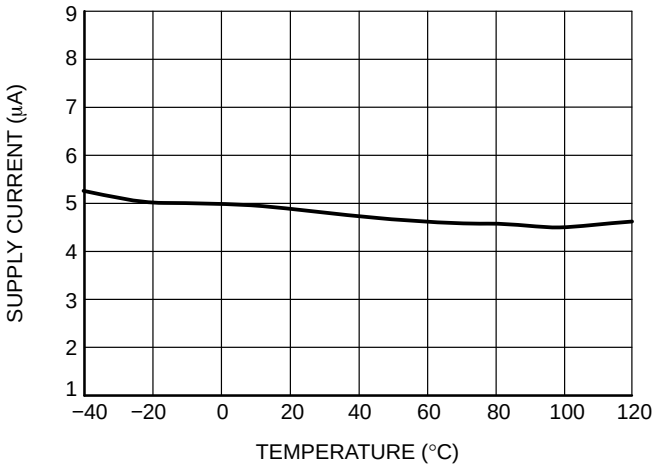

Figure 2. V_{CC} Supply Current vs. Temperature

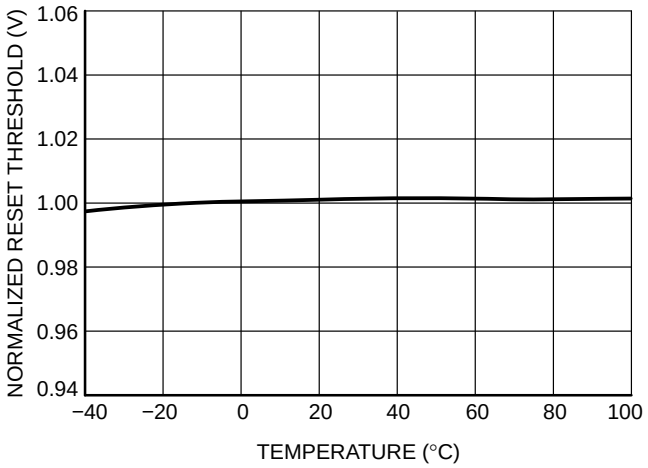

Figure 3. Normalized Reset Threshold Voltage vs. Temperature

FUNCTIONAL DESCRIPTION

Processor RESET

The CAT823 detects supply voltage (V_{CC}) conditions that are below the specified voltage trip value (V_{RST}) and provide a reset output to maintain correct system operation. On power−up, $\overline{\text{RESET}}$ (and RESET if available) are kept active for a minimum delay t_{RP} of 140 ms after the supply voltage (V_{CC}) rises above V_{RST} to allow the power supply and processor to stabilize. When V_{CC} drops below the voltage trip value (V_{RST}), the reset output signals $\overline{\text{RESET}}$ (and RESET) are pulled active. $\overline{\text{RESET}}$ (and RESET if available) is specifically designed to provide the reset input signals for processors. This provides reliable and consistent operation as power is turned on, off or during brownout conditions by maintaining the processor operation in known conditions.

Manual RESET

The CAT823 has a Manual Reset ($\overline{\text{MR}}$) input to allow for alternative control of the reset outputs. The $\overline{\text{MR}}$ input is designed for direct connection to a pushbutton (see Figure 4). The $\overline{\text{MR}}$ input is internally pulled up by 52 kΩ resistor and must be pulled low to cause the reset outputs to go active. Internally, this input is debounced and timed such that $\overline{\text{RESET}}$ (and RESET) signals of at least 140 ms minimum will be generated. The min 140 ms t_{RP} delay commences as the Manual Reset input is released from the low level (see Figure 5).

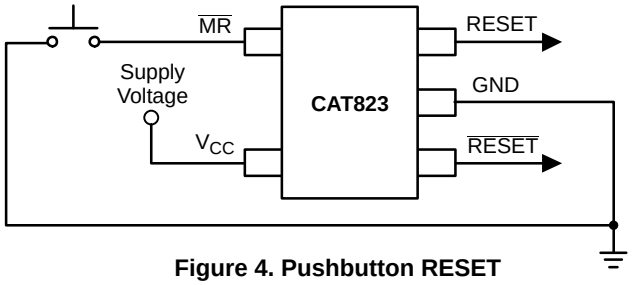

Figure 4. Pushbutton RESET

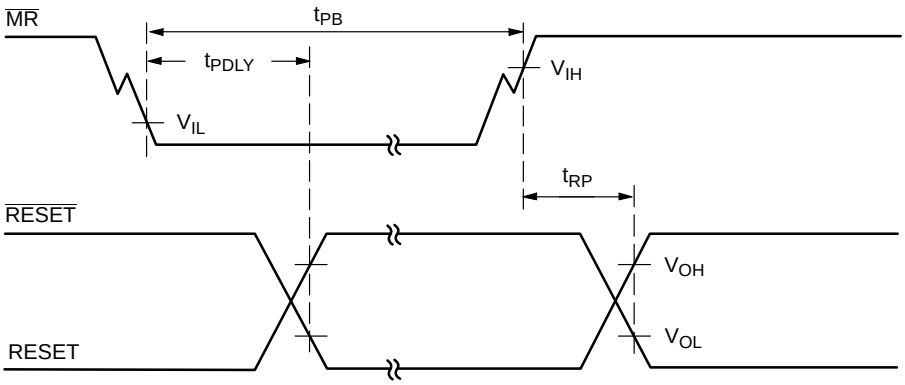

Figure 5. Timing Diagram – Pushbutton RESET

Watchdog Timer

The CAT823 and CAT824 provide a Watchdog input (WDI). The watchdog timer function forces $\overline{\text{RESET}}$ (and RESET in the CAT824) signals active when the WDI input does not have a transition from low−to−high or high−to−low within 1.12 seconds. Timeout of the watchdog starts when $\overline{\text{RESET}}$ (RESET on the CAT824) becomes inactive. If a transition occurs on the WDI input pin prior to the watchdog time−out, the watchdog timer is reset and begins to time−out again. If the watchdog timer is allowed to time−out, then the reset output(s) will go active for t_{RP} and once released will repeat the watchdog timeout process.

Figure 6 below shows a typical implementation of a watchdog function. Any processor signal that repeats dependant on the normal operation of the processor or directed by the software operating on the processor can be used to strobe the watchdog input. The most reliable is a dedicated I/O output transitioned by a specific software instruction.

The watchdog can be disabled by floating (or tri−stating) the WDI input (see Figure 7). If the watchdog is disabled the WDI pin will be pulled low for the first 7/8th's of the watchdog period (t_{WD}) and pulled high for the last 1/8th of the watchdog period. This pulling low of the WDI input and then high is used to detect an open or tri−state condition and will continue to repeat until the WDI input is driven high or low.

For most efficient operation of devices with the watchdog function the WDI input should be held low the majority of the time and only strobed high as required to reset the watchdog timer.

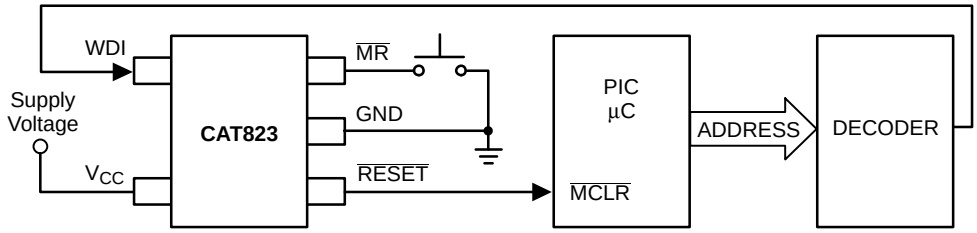

Figure 6. Watchdog Timer

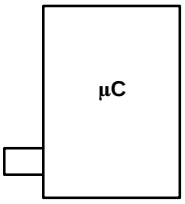

Figure 7. Watchdog Disable Circuit

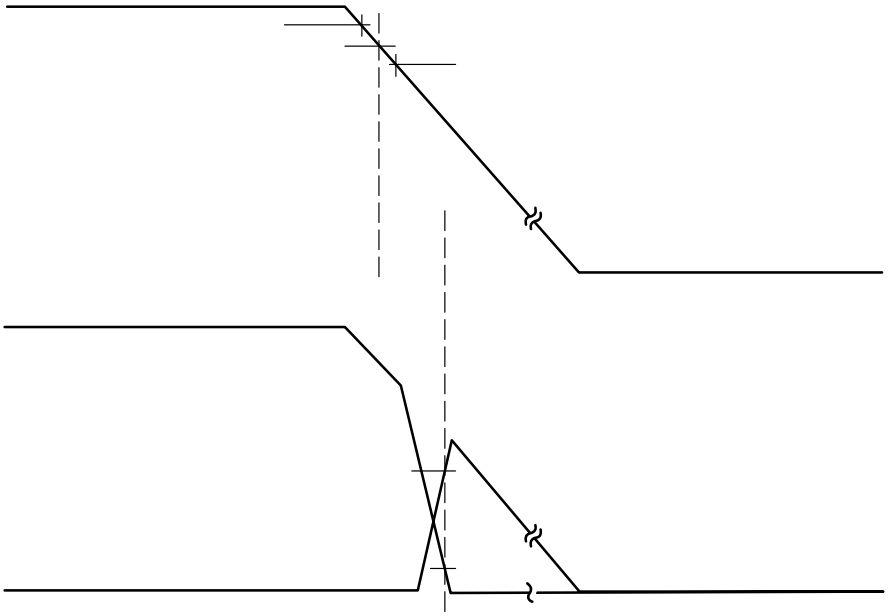

Figure 9. Timing Diagram – Power Down

Application Notes

µP's with Bidirectional Reset Pins

The $\overline{\text{RESET}}$ output can be pulled low by processors like the 68HC11 allowing for a system reset issued by the processor. The maximum pullup current that can be sourced by the CAT82_M is 1.5 mA (and by the CAT82_T/R/S/Z/Y is 800 µA) allowing the processor to pull the output low even when the CAT82x is pulling it high.

Power Transients

Generally short duration negative−going transients of less than 2 µs on the power supply at V_{RST} minimum will not cause a reset condition. However the lower the voltage of the transient the shorter the required time to cause a reset output. These issues can usually be remedied by the proper location of bypass capacitance on the circuit board.

Output Valid Conditions

The $\overline{\text{RESET}}$ output uses a push−pull output which can maintain a valid output down to a V_{CC} of 1.0 volts. To sink current below 0.8 V a resistor can be connected from $\overline{\text{RESET}}$ to Ground (see Figure 11.) This arrangement will maintain a valid value on the $\overline{\text{RESET}}$ output during both power up and down but will draw current when the $\overline{\text{RESET}}$ output is in the high state. A resistor value of about 100 kΩ should be adequate in most situations to maintain a low condition valid output down to V_{CC} equal to 0 V.

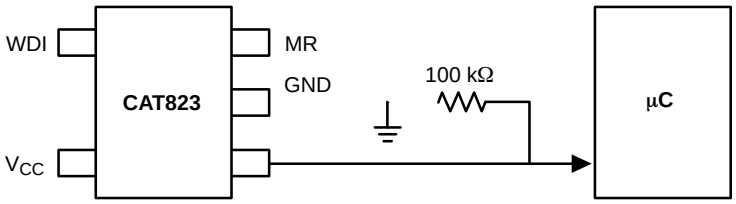

Figure 11. $\overline{\text{RESET}}$ Valid to 0 Volts V_{CC}

ORDERING INFORMATION

Order Number		Top Mark	Inputs		Outputs			
NiPdAu	Voltage	NiPdAu	MR	WDI	$\overline{\text{RESET}}$	RESET	Package	Shipping[†]
CAT823TTDI−GT3	3.08 V	ETA	*	*	*		TSOT−23−5	3,000 / Tape & Reel

DISCONTINUED (Note 9)

CAT823STDI−GT3	2.93 V	ETA	*	*	*		TSOT−23−5	3,000 / Tape & Reel
CAT823RTDI−GT3	2.63 V	ETA						

TSOT−23, 5 LEAD
CASE 419AE−01
ISSUE O

DATE 19 DEC 2008