

http://onsemi.com



SOIC-8 V SUFFIX CASE 751BD

PIN CONFIGURATION

 \bigcirc

- Low Output Resistance, 10Ω Max.
- High Power Efficiency
- Selectable Charge Pump Frequency of 25 kHz or 135 kHz; Optimize Capacitor Size
- Low Quiescent Current
- Pin-compatible to MAX660, LTC660 with Higher Frequency Operation
- Available in 8–pin SOIC Package
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Negative Voltage Generator
- Voltage Doubler
- Voltage Splitter
- Low EMI Power Source
- GaAs FET Biasing
- Lithium Battery Power Supply
- Instrumentation
- LCD Contrast Bias
- Cellular Phones, Pagers

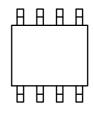


Table 2. ABSOLUTE MAXIMUM RATINGS

Parameters	Ratings	Units
V+ to GND	6	V
Input Voltage (Pins 1, 6 and 7)	-0.3 to (V+ + 0.3)	V
BOOST/FC and OSC Input Voltage	The least negative of (Out – 0.3 V) or $(V+ - 6 V)$ to $(V+ + 0.3 V)$	V
Output Short–circuit Duration to GND (OUT may be shorted to GND for 1 sec without damage but shorting OUT to V+ should be avoided.)	1	sec.
Continuous Power Dissipation (T _A = 70°C) Plastic DIP SO TDFN	730 500 1	mW mW W
Storage Temperature	-65 to +160	°C
Lead Soldering Temperature (10 sec)	300	°C
ESD Rating – Human Body Model	2000	V
Operating Ambient Temperature Range	-40 to +85	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

NOTE: T_A = Ambient Temperature

Table 3. ELECTRICAL CHARACTERISTICS (V+ = 5 V, C1 = C2 = 100 μ F, Boost/FC = Open, C_{OSC} = 0 pF, and Test Circuit is Figure 3 unless otherwise noted. Temperature is T_A = T_{AMIN} to T_{AMAX} unless otherwise noted.)

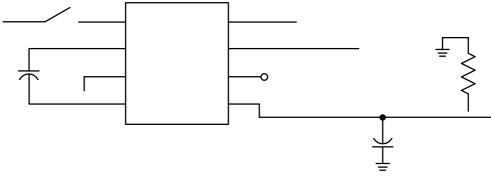
Parameter	Symbol	Conditions	Min	Тур	Max	Units
Supply Voltage	VS	Inverter: LV = Open, $R_L = 1 \ k\Omega$	3.0		5.5	V
		Inverter: LV = GND, $R_L = 1 k\Omega$	1.5		5.5	
		Doubler: LV = OUT, R_L = 1 k Ω	2.5		5.5	
Supply Current	IS	BOOST/FC = open, LV = Open		0.2	0.5	mA
		BOOST/FC = V+, LV = Open		1	3	
Output Current	IOUT	OUT is more negative than -4 V	100			mA
Output Resistance	RO	$\begin{array}{l} \text{C1}=\text{C2}=10 \ \mu\text{F} \\ \text{BOOST/FC}=\text{V+} \ (\text{C1}, \ \text{C2} \ \text{ESR} \leq 0.5 \ \Omega) \end{array}$		3.5	10	Ω
		C1 = C2 = 100 µF (Note 5)		3.5	10	
Oscillator Frequency	FOSC	BOOST/FC = Open	10	25		kHz
(Note 6)		BOOST/FC = V+	80	135		
OSC Input Current	IOSC	BOOST/FC = Open BOOST/FC = V+		±2 ±10		μΑ
Power Efficiency	PE	$R_L = 1 \ k\Omega$ connected between V+ and OUT, $T_A = 25^{\circ}C$ (Doubler)	96	98		%
		R_{L} = 500 Ω connected between GND and OUT, T_{A} = 25°C (Inverter)	92	96		
		I_L = 100 mA to GND, T_A = 25°C (Inverter)		88		
Voltage Conversion Efficiency	VEFF	No load, $T_A = 25^{\circ}C$	99	99.9		%

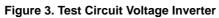
4. In Figure 3, test circuit electrolytic capacitors C1 and C2 are 100 μF and have 0.2 Ω maximum ESR. Higher ESR levels may reduce efficiency and output voltage.

5. The output resistance is a combination of the internal switch resistance and the external capacitor ESR. For maximum voltage and efficiency keep external capacitor ESR under 0.2 Ω.

 FOSC is tested with C_{OSC} = 100 pF to minimize test fixture loading. The test is correlated back to C_{OSC} = 0 pF to simulate the capacitance at OSC when the device is inserted into a test socket without an external C_{OSC}.

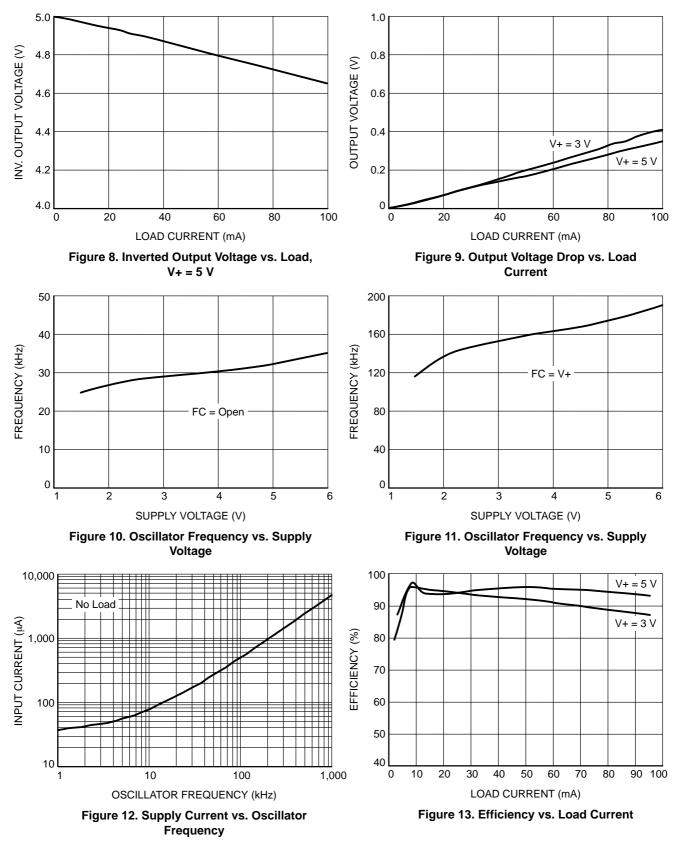
Voltage Inverter



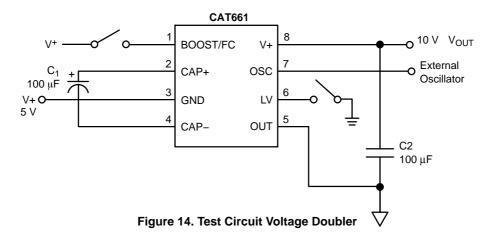


CAT661



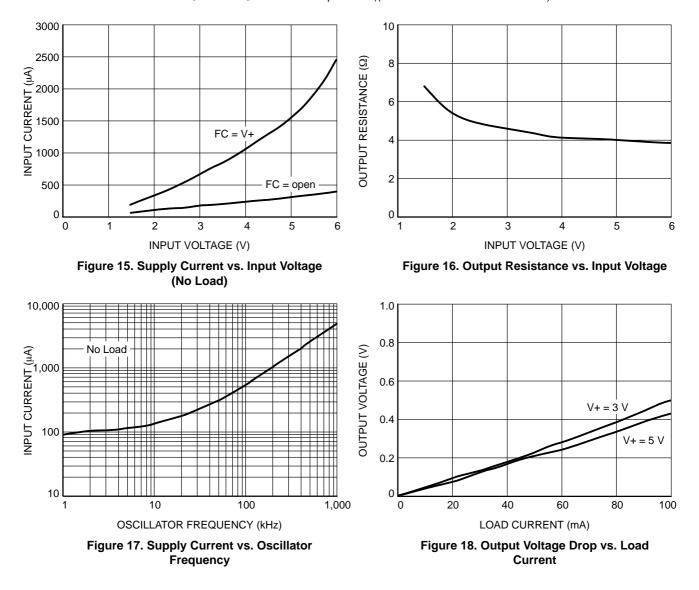


Voltage Doubler



TYPICAL OPERATING CHARACTERISTICS

⁽Typical characteristic curves are generated using the circuit in Figure 14. Doubler test conditions are: V+ = 5 V, LV = GND, BOOST/FC = Open and $T_A = 25^{\circ}C$ unless otherwise indicated.)



Application Information

Circuit Description and Operating Theory

The CAT661 switches capacitors to invert or double an input voltage.

Figure 19 shows a simple switch capacitor circuit. In position 1 capacitor C1 is charged to voltage V1. The total charge on C1 is Q1 = C1V1. When the switch moves to position 2, the input capacitor C1 is discharged to voltage V2. After discharge, the charge on C1 is Q2 = C1V2.

The charge transferred is:

$$\Delta Q = Q1 - Q2 = C1 \times (V1 - V2)$$

If the switch is cycled "F" times per second, the current (charge transfer per unit time) is:

$$I = F \times \Delta Q = F \times C1 (V1 - V2)$$

Rearranging in terms of impedance:

$$I = \frac{(V1 - V2)}{(1/FC1)} = \frac{V1 - V2}{REQ}$$

The 1/FC1 term can be modeled as an equivalent impedance REQ. A simple equivalent circuit is shown in

Figure 20. This circuit does not include the switch resistance nor does it include output voltage ripple. It does allow one to understand the switch–capacitor topology and make prudent engineering tradeoffs.

For example, power conversion efficiency is set bjET0 G..0001 2d as The 1/F, willpleminat inclunclude 5 Tw[im, as 8588usngie total)**TT***

Oscillator Frequency Control

The switching frequency can be raised, lowered or driven from an external source. Figure 22 shows a functional diagram of the oscillator circuit.

The CAT661 oscillator has four control modes:

Table 4.

BOOST/FC Pin Connection

Capacitor Selection

Low ESR capacitors are necessary to minimize voltage losses, especially at high load currents. The exact values of C1 and C2 are not critical but low ESR capacitors are necessary.

The ESR of capacitor C1, the pump capacitor, can have a pronounced effect on the output. C1 currents are approximately twice the output current and losses occur on both the charge and discharge cycle. The ESR effects are thus multiplied by four. A 0.5 Ω ESR for C1 will have the same effect as a 2 Ω increase in CAT661 output impedance.

Output voltage ripple is determined by the value of C2 and the load current. C2 is charged and discharged at a current roughly equal to the load current. The internal switching frequency is one-half the oscillator frequency.

 $VRIPPLE = IOUT/(FOSC \times C2) + IOUT \times ESRC2$

For example, with a 25 kHz oscillator frequency (12.5 kHz switching frequency), a 150 μ F C2 capacitor with an ESR of 0.2 Ω and a 100 mA load peak–to–peak ripple voltage is 45 mV.

Table 5. VRIPPLE vs. FOSC

VRIPPLE (mV) IOUT (mA)		FOSC (kHz)	C2 (µF)	C2 ESR (Ω)
45	100	25		

Capacitor Suppliers

The following manufacturers supply low-ESR capacitors:

Table 6. CAPACITOR SUPPLIERS

Manufacturer	Capacitor Type	Phone	WEB	Email	Comments
AVX/Kyocera	TPS/TPS3	843-448-9411	www.avxcorp.com	avx@avxcorp.com	Tantalum
Vishay/Sprague	595	402-563-6866	www.vishay.com	-	Aluminum
Sanyo	MV–AX, UGX	619–661–6835	www.sanyo.com	Svcsales@sanyo.com	Aluminum
Nichicon	F55	847-843-7500	www.nichicon-us.com	-	Tantalum
	HC/HD				Aluminum

Capacitor manufacturers continually introduce new series and offer different package styles. It is recommended that before a design is finalized capacitor manufacturers should be surveyed for their latest product offerings.

Controlling Loss in CAT661 Applications

There are three primary sources of voltage loss:

1. Output resistance:

VLOSS = ILOAD x ROUT, where ROUT is the CAT661 output resistance and ILOAD is the load current.

2. Charge pump (C1) capacitor ESR:

VLOSSC1 \approx 4 x ESRC1 x ILOAD, where ESRC1 is the ESR of capacitor C1. 3. Output or reservoir (C2) capacitor ESR:

VLOSSC2 = ESRC2 x ILOAD, where ESRC2 is the ESR of capacitor C2.

Increasing the value of C2 and/or decreasing its ESR will reduce noise and ripple.

The effective output impedance of a CAT661 circuit is approximately:

Rcircuit \approx Rout 661 + (4 × ESRC1) + ESRC2

Typical Applications

Voltage Inversion Positive-to-Negative

CAT661

Precision Voltage Divider

A precision voltage divider is shown in Figure 26. With load currents under 100 nA, the voltage at pin 2 will be within 0.002% of V+/2.

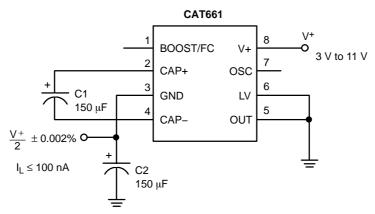
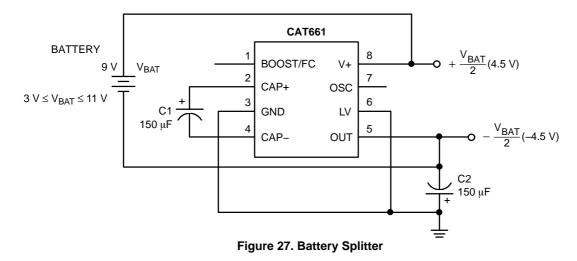


Figure 26. Precision Voltage Divider (Load ≤ 100 nA)

Battery Voltage Splitter

Positive and negative voltages that track each other can be obtained from a battery. Figure 27 shows how a 9 V battery can provide symmetrical positive and negative voltages equal to one-half the battery voltage.



CAT661

Cascade Operation for Higher Negative Voltages

The CAT661 can be cascaded as shown in Figure 28 to generate more negative voltage levels. The output resistance is approximately the sum of the individual CAT661 output resistance.

 V_{OUT} = -N x V_{IN}, where N represents the number of cascaded devices.

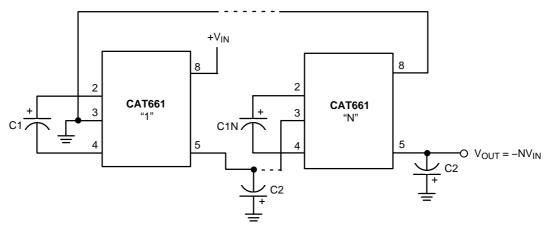
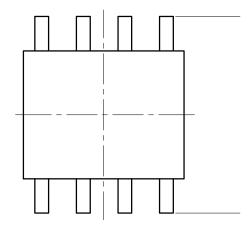


Figure 28. Cascading to Increase Output Voltage

Parallel Operation

SOIC-8, 150 mils CASE 751BD ISSUE O

DATE 19 DEC 2008





onsemi, , and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "onsemi" or its affiliates and/or subsidiaries in the United States and/or other countries. onsemi owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of onsemi's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. Onsemi reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and onsemi makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or incruit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using onsemi