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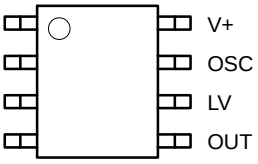
SOIC−8
V SUFFIX
CASE 751BD

PIN CONFIGURATION



(Top View)

- Available in 8−pin SOIC Package
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Negative Voltage Generator
- Voltage Doubler
- Voltage Splitter
- Low EMI Power Source
- GaAs FET Biasing
- Lithium Battery Power Supply
- Instrumentation
- LCD Contrast Bias
- Cellular Phones, Pagers

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Typical Application

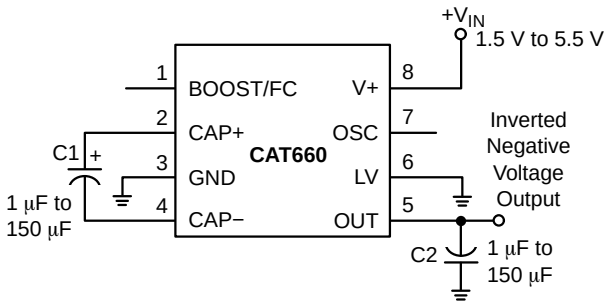

Figure 1. Voltage Inverter

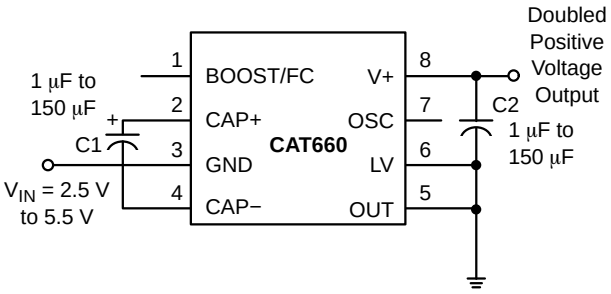

Figure 2. Positive Voltage Doubler

Table 1. PIN DESCRIPTIONS

Pin Number	Name	Inverter Mode	Doubler Mode
1	Boost/FC		

Table 2. ABSOLUTE MAXIMUM RATINGS

Parameters	Ratings	Units
V+ to GND	6	V
Input Voltage (Pins 1, 6 and 7)	−0.3 to (V+ + 0.3)	V
BOOST/FC and OSC Input Voltage	The least negative of (Out − 0.3 V) or (V+ − 6 V) to (V+ + 0.3 V)	V
Output Short−circuit Duration to GND (OUT may be shorted to GND for 1 sec without damage but shorting OUT to V+ should be avoided.)	1	sec.
Continuous Power Dissipation (T_A = 70°C) Plastic DIP SOIC TDFN	 730 500 1	 mW mW W
Storage Temperature	−65 to +160	°C
Lead Soldering Temperature (10 sec)	300	°C
Operating Ambient Temperature Range	−40 to +85	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

NOTE: T_A = Ambient Temperature

Table 3. ELECTRICAL CHARACTERISTICS (V+ = 5 V, C1 = C2 = 150 μF, Boost/FC = Open, C_{OSC} = 0 pF, inverter mode with test circuit as shown in Figure 3 unless otherwise noted. Temperature is over operating ambient temperature range unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Voltage	VS	Inverter: LV = Open, R_L = 1 kΩ	3.0		5.5	V
		Inverter: LV = GND, R_L = 1 kΩ	1.5		5.5	
		Doubler: LV = OUT, R_L = 1 kΩ	2.5		5.5	
Supply Current	IS	BOOST/FC = open, LV = Open		0.09	0.5	mA
		BOOST/FC = V+, LV = Open		0.3	3	
Output Current	IOUT	OUT is more negative than −4 V	100			mA
Output Resistance	RO	I_L = 100 mA, C1 = C2 = 150 μF (Note 5) BOOST/FC = V+ (C1, C2 ESR ≤ 0.5 Ω)		4	7	Ω
		I_L = 100 mA, C1 = C2 = 10 μF			12	
Oscillator Frequency (Note 6)	FOSC	BOOST/FC = Open	5	10		kHz
		BOOST/FC = V+	40	80		
OSC Input Current	IOSC	BOOST/FC = Open BOOST/FC = V+		±1 ±5		μA
Power Efficiency	PE	R_L = 1 kΩ connected between V+ and OUT, T_A = 25°C (Doubler)	96	98		%
		R_L = 500 Ω connected between GND and OUT, T_A = 25°C (Inverter)	92	96		
		I_L = 100 mA to GND, T_A = 25°C (Inverter)		88		
Voltage Conversion Efficiency	VEFF	No load, T_A = 25°C	99	99.9		%

4. In Figure 3, test circuit capacitors C1 and C2 are 150 μF and have 0.2 Ω maximum ESR. Higher ESR levels may reduce efficiency and output voltage.
5. The output resistance is a combination of the internal switch resistance and the external capacitor ESR. For maximum voltage and efficiency keep external capacitor ESR under 0.2 Ω.
6. FOSC is tested with C_{OSC} = 100 pF to minimize test fixture loading. The test is correlated back to C_{OSC} = 0 pF to simulate the capacitance at OSC when the device is inserted into a test socket without an external C

Voltage Inverter

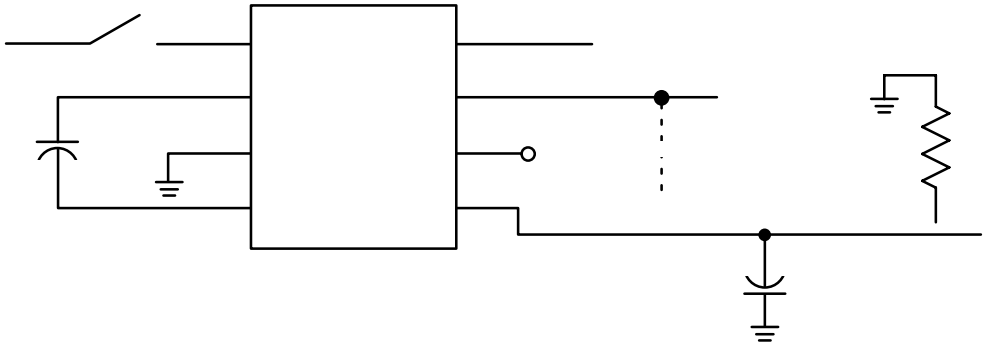

Figure 3. Test Circuit

TYPICAL OPERATING CHARACTERISTICS

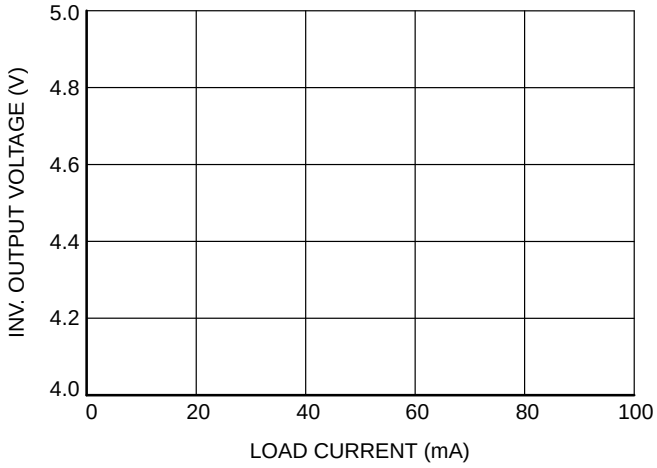

Figure 8. Inverted Output Voltage vs. Load, V+ = 5 V

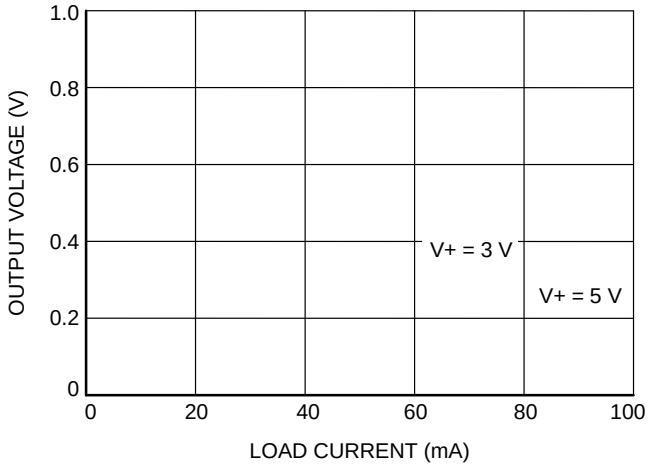

Figure 9. Output Voltage Drop vs. Load Current

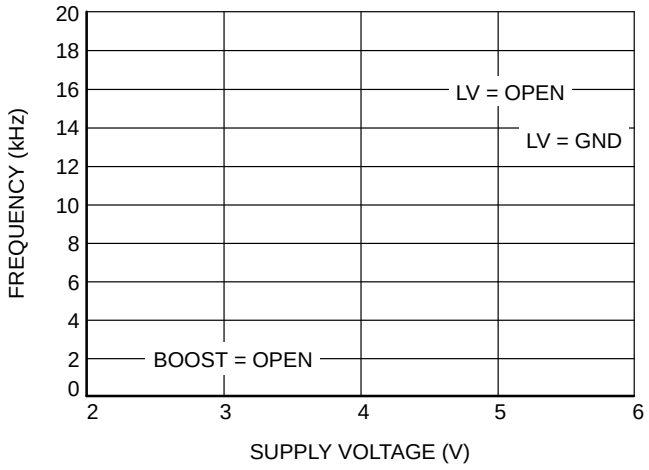

Figure 10. Oscillator Frequency vs. Supply Voltage

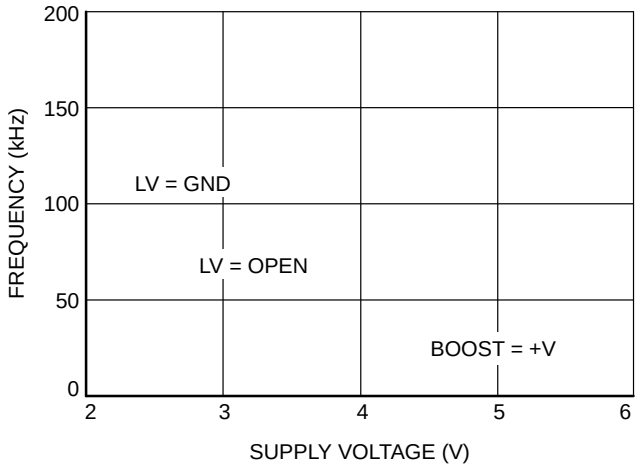

Figure 11. Oscillator Frequency vs. Supply Voltage

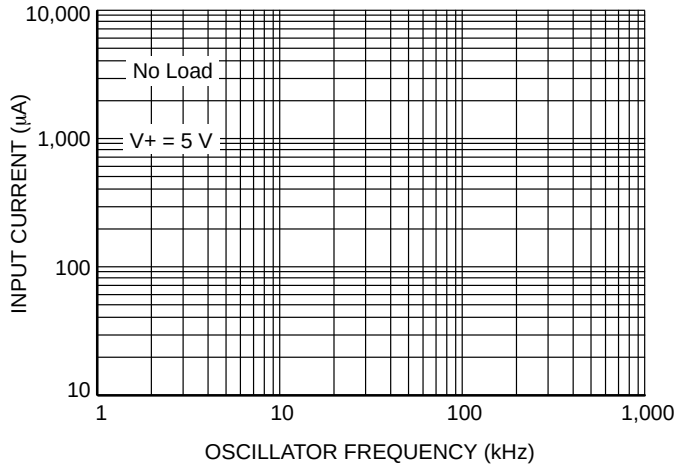

Figure 12. Supply Current vs. Oscillator Frequency

Application Information

Circuit Description and Operating Theory

The CAT660 switches capacitors to invert or double an input voltage.

Figure 13 shows a simple switch capacitor circuit. In position 1 capacitor C1 is charged to voltage V1. The total charge on C1 is Q1 = C1V1. When the switch moves to position 2, the input capacitor C1 is discharged to voltage V2. After discharge, the charge on C1 is Q2 = C1V2.

The charge transferred is:

$$\Delta Q = Q1 - Q2 = C1 \times (V1 - V2)$$

If the switch is cycled “F” times per second, the current (charge transfer per unit time) is:

$$I = F \times \Delta Q = F \times C1\,(V1 - V2)$$

Rearranging in terms of impedance:

$$I = \frac{(V1 - V2)}{(1/FC1)} = \frac{V1 - V2}{REQ}$$

The 1/FC1 term can be modeled as an equivalent impedance REQ. A simple equivalent circuit is shown in Figure 14. This circuit does not include the switch resistance nor does it include output voltage ripple. It does allow one to understand the switch−capacitor topology and make prudent engineering tradeoffs.

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Oscillator Frequency Control

The switching frequency can be raised, lowered or driven from an external source. Figure 16 shows a functional diagram of the oscillator circuit.

The CAT660 oscillator has four control modes:

Table 4.

BOOST/FC Pin Connection	OSC Pin Connection	Nominal Oscillator Frequency
Open	Open	10 kHz
BOOST/FC = V+	Open	80 kHz
Open or		

Capacitor Selection

Low ESR capacitors are necessary to minimize voltage losses, especially at high load currents. The exact values of C1 and C2 are not critical but low ESR capacitors are necessary.

The ESR of capacitor C1, the pump capacitor, can have a pronounced effect on the output. C1 currents are approximately twice the output current and losses occur on both the charge and discharge cycle. The ESR effects are thus multiplied by four. A 0.5 Ω ESR for C1 will have the same effect as a 2 Ω increase in CAT660 output impedance.

Output voltage ripple is determined by the value of C2 and the load current. C2 is charged and discharged at a current roughly equal to the load current. The internal switching frequency is one−half the oscillator frequency.

$$VRIPPLE = IOUT/(FOSC \times C2) + IOUT \times ESRC2$$

For example, with a 10 kHz oscillator frequency (5 kHz switching frequency), a 150 μF C2 capacitor with an ESR of 0.2 Ω and a 100 mA load peak−to−peak ripple voltage is 87 mV.

Table 5. VRIPPLE vs. FOSC

VRIPPLE (mV)	IOUT (mA)	FOSC (kHz)	C2 (μF)	C2 ESR (Ω)
87	100	10	150	0.2
28	100	80	150	0.2

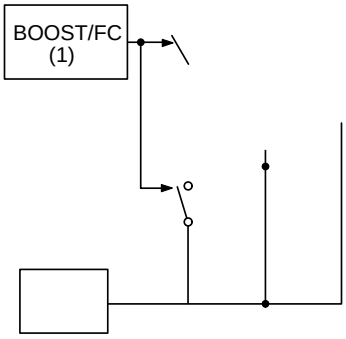

Figure 16. Oscillator

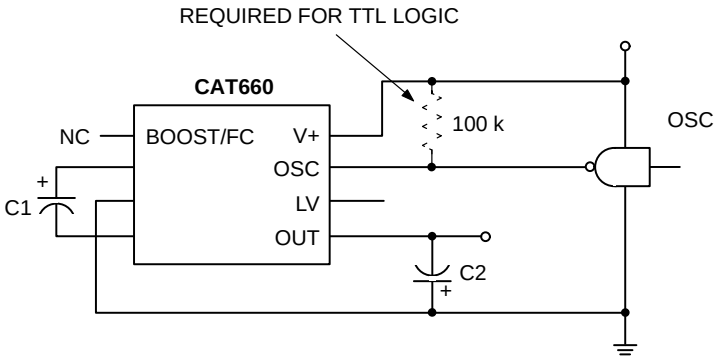

Figure 17. External Clocking

Typical Applications

Voltage Inversion Positive−to−Negative

Precision Voltage Divider

A precision voltage divider is shown in Figure 20. With very light load currents under 100 nA, the voltage at pin 2 will be within 0.002% of V+/2. Output voltage accuracy decreases with increasing load.

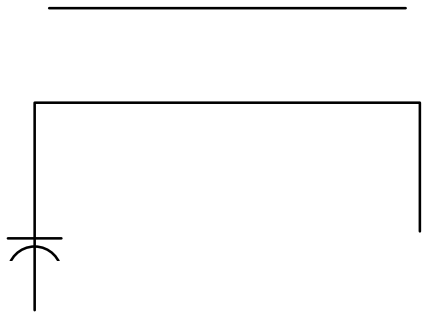

Figure 20. Precision Voltage Divider (Load ≤ 100 nA)

SOIC−8, 150 mils
CASE 751BD
ISSUE O

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