3-Channel Constant-Current RGB LED Driver with Individual PWM Dimming

CAT4109, CAV4109

Description

The CAT4109/CAV4109 is a 3-channel constant-current LED driver, requiring no inductor. LED channel currents up to 175 mA are programmed independently via separate external resistors. Low output voltage operation of 0.4 V at 175 mA allows for more power efficient designs across wider supply voltage range. The three LED pins are compatible with high voltage up to 25 V supporting applications with long strings of LEDs.

Three independent control inputs PWM1, PWM2, PWM3, control respectively LED1, LED2, LED3 channels. The device also includes an output enable (OE) control pin to disable all three channels independently of the PWMx input states.

Thermal shutdown protection is incorporated in the device to disable the LED outputs whenever the die temperature exceeds 150°C. The device is available in a 16-lead SOIC package.

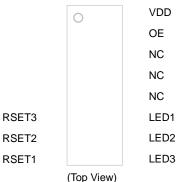
Features

- 3 Independent Current Sinks up to 175 mA rated 25 V
- LED Current Set by External Low Power Control Resistors
- Individual PWM Control per Channel
- Low Dropout Current Source (0.4 V at 175 mA)
- Output Enable Input for Dimming
- "Zero" Current Shutdown Mode
- 3 V to 5.5 V Logic Supply
- Thermal Shutdown Protection
- 16–lead SOIC Package
- CAV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

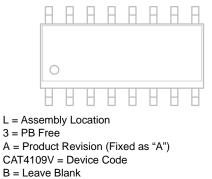
Application

- Multi-color LED, Architectural Lighting
- LED Signs and Displays
- LCD Backlight





MARKING DIAGRAM



B = Leave Blank

- Y = Production Year (Last Digit)
- M = Production Month (1-9, O, N, D)
- XXXX = Last Four Digits of Assembly Lot Number

CAV4109V-GT2 SOIC-16 3,000/ (Note 1) (Pb-Free) Tape & Reel

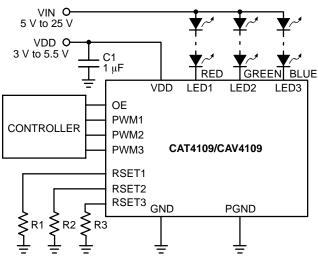


Figure 1. Typical Application Circuit

Table 1. ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Units
VDD Voltage	6	V
Input Voltage Range (OE, PWM1, PWM2, PWM3)	–0.3 V to 6 V	V
LED1, LED2, LED3 Voltage	25	V
DC Output Current on LED1 to LED3	200	mA
Storage Temperature Range	–55 to +160	°C
Junction Temperature Range	-40 to +150	°C
Lead Soldering Temperature (10 sec.)	300	°C
ESD RATING		

Human Body Model (Note 2) LV pins (non LEDn pins # 3, 4, 5, 6, 7, 8, 15 and 16) HV pins(LEDn pins #9, 10 and 11)	1500 500	V
Machine Model (Note 3) LV pins (non LEDn pins # 3, 4, 5, 6, 7, 8, 15 and 16) HV pins (LEDn pins #9, 10 and 11)	200 175	V
Charged Device Model (Note 4)	1000	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device function

Table 3. ELECTRICAL OPERATING CHARACTERISTICS (Min and Max values are over recommended operating conditions	
unless specified otherwise. Typical values are at V_{DD} = 5.0 V, T_{AMB} = 25°C.)	

Symbol	Name	Conditions	Min	Тур	Max	Units
DC CHARA	CTERISTICS		•		•	
I _{DD1}	Supply Current Outputs Off	V_{LED} = 5 V, R_{SET} = 24.9 k Ω		2	5	mA
I _{DD2}	Supply Current Outputs Off	V_{LED} = 5 V, R_{SET} = 5.23 k Ω		4	10	mA
I _{DD3}	Supply Current Outputs On	V_{LED} = 0.5 V, R_{SET} = 24.9 k Ω		2	5	mA
I _{DD4}	Supply Current Outputs On	V_{LED} = 0.5 V, R_{SET} = 5.23 k Ω		4	10	mA
I _{SHDN}	Shutdown Current	V _{OE} = 0 V			1	μΑ
I _{LKG}	LED Output Leakage	V _{LED} = 5 V, Outputs Off	–1		1	μΑ
R _{OE}	OE Pull-down Resistance		140	190	250	kΩ
V _{OE_IH} V _{OE_IL}	OE Logic High Level OE Logic Low Level		1.3		0.4	V
V _{PWM_IH} V _{PWM_IL}	PWMx Logic High Level PWMx Logic Low Level		0.7 x V _{DD}		0.3 x V _{DD}	V
۱ _{IL}	Logic Input Leakage Current (PWMx)	$V_{PWMx} = V_{DD}$ or GND	-5	0	5	μΑ
V _{RSETx}	RSETx Regulated Voltage		1.17	1.2	1.23	V
T _{SD}	Thermal Shutdown			150		°C
T _{HYS}	Thermal Hysteresis			20		°C
I _{LED} /I _{RSET}	RSET to LED Current Gain Ratio	100 mA LED Current		400		
V _{UVLO}	Undervoltage Lockout (UVLO) Threshold			1.8		V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Table 4. RECOMMENDED TIMING (Min and Max values are over recommended operating conditions unless specified otherwise.Typical values are at $V_{DD} = 5.0 \text{ V}$, $T_{AMB} = 25^{\circ}$ C.)

Symbol	Name	Conditions	Min	Тур	Max	Units
t _{PS}	Turn–On time, OE rising to I _{LED} from Shutdown	I _{LED} = 100 mA		1.4		μs
t _{P1}	Turn–On time, OE or PWMx rising to I _{LED}	I _{LED} = 100 mA		600		ns
t _{P2}	Turn–Off time, OE or PWMx falling to I _{LED}	I _{LED} = 100 mA		300		ns
t _R	LED rise time	I _{LED} = 100 mA		300		ns
t _F	LED fall time	I _{LED} = 100 mA		300		ns
t _{LO}	OE low time		1			μs
t _{HI}	OE high time		5			μs
t _{PWRDWN}	OE low time to shutdown delay			4	8	ms

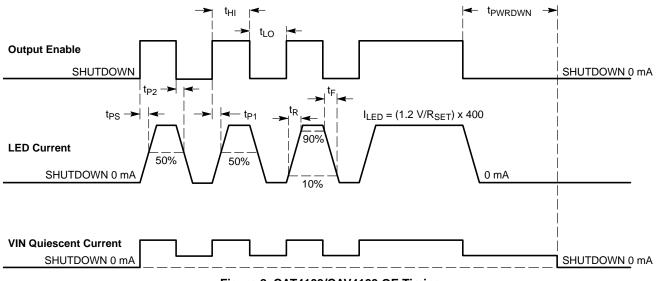


Figure 2. CAT4109/CAV4109 OE Timing

OE Operation

The Output Enable (OE) pin has two primary functions. When the OE input goes from high to low, all three LED channels are turned off. If OE remains low for longer than t_{PWRDWN} , the device enters shutdown mode drawing "zero current" from the supply.

The OE input can be used to adjust the contrast of the RGB LED by applying an external PWM signal. The device has a very fast turn–on time (from OE rising to LED on) allowing "instant on" when dimming LEDs.

When applying PWM signals to the three PWMx inputs and using the OE pin for dimming, the OE PWM frequency should be much lower to preserve the color mixing. Accurate linear dimming on OE is compatible with PWM frequencies from 100 Hz to 5 kHz for PWM duty cycle down to 1%. PWM frequencies up to 50 kHz can be supported for duty cycles greater than 10%.

When performing a combination of low frequencies and small duty cycles, the device may enter shutdown mode. This has no effect on the dimming accuracy, because the turn–on time t_{PS} is very short, in the range of 1 µs.

To ensure that PWM pulses are recognized, pulse width low time t_{LO} should be longer than 1 µs. The driver enters a "zero current" shutdown mode after a 4 ms delay (typical) when OE is held low.

TYPICAL PERFORMANCE CHARACTERISTICS

 $(V_{IN}$

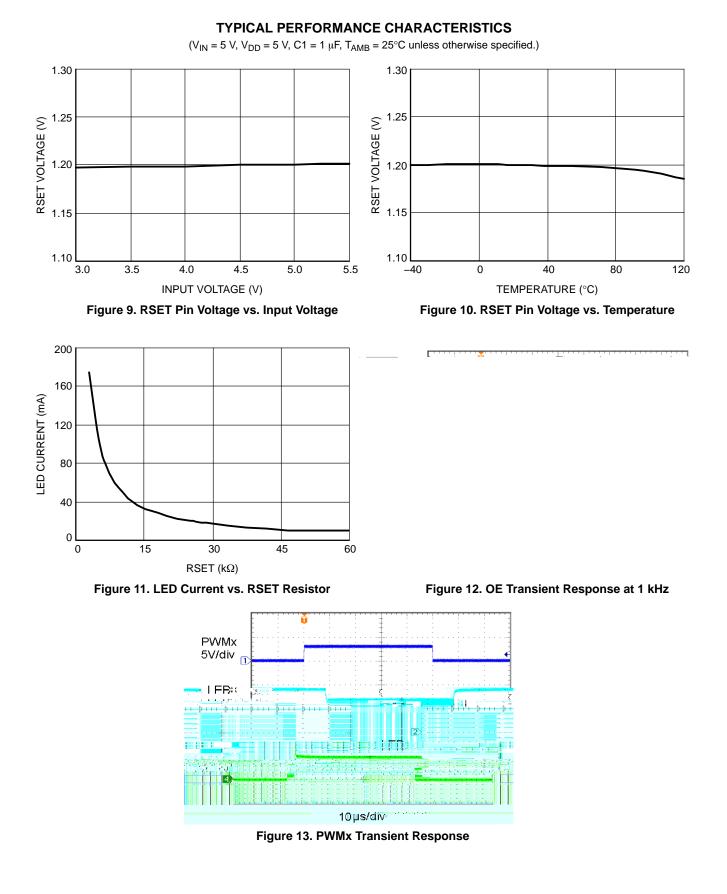
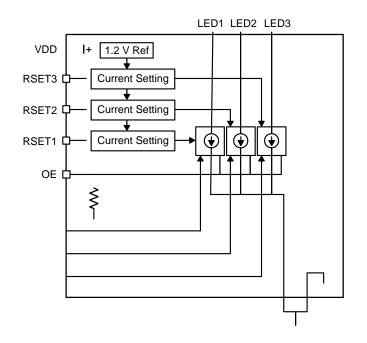


Table 5. PIN DESCRIPTIONS

	Name	Pin Number	Function
ſ	PGND	1	

BLOCK Diagram



Application Information

Power Dissipation

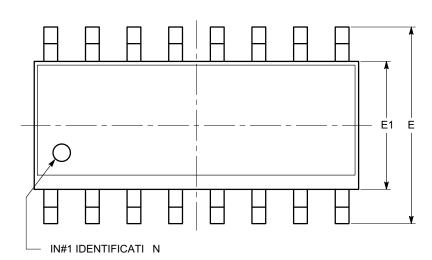
The power dissipation (P_D) of the CAT4109/CAV4109 can be calculated as follows:

$$\mathbf{P}_{\mathrm{D}} = \left(\mathbf{V}_{\mathrm{DD}} \times \mathbf{I}_{\mathrm{DD}}\right) + \Sigma \left(\mathbf{V}_{\mathrm{LEDN}}\right)$$

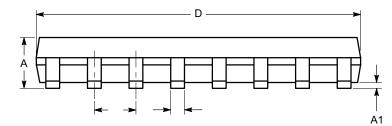
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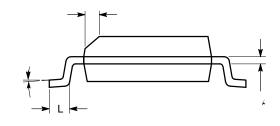
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TOP VIEW





END VIEW

SIDE VIEW

Notes:

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