CAT4103

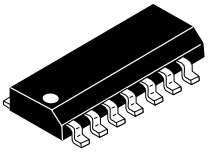
3-Channel Constant-Current RGB LED Driver

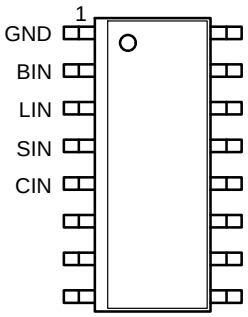
The CAT4103 is a 3 channel, linear based constant current LED driver designed for RGB LED control, requiring no inductor and provides a low noise operation. LED channel currents up to 175 mA are programmed independently via separate external resistors. Low output voltage operation of 0.4 V at 175 mA allows for more power efficient designs across wider supply voltage range. The three LED pins are compatible with high voltage up to 25 V supporting applications with long strings of LEDs.

A high speed 4 wire 25 MHz serial interface controls each individual channel using a shift register and latch configuration. Output data pins allow multiple devices to be cascaded and programmed via one serial interface with no need for external drivers or timing considerations. The device also includes a blanking control pin (BIN) that can be used to disable all channels independently of the interface.

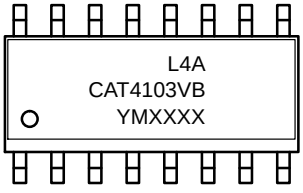
Thermal shutdown protection is incorporated in the device to disable the LED outputs whenever the die temperature exceeds 150°C.

The device is available in a 16 lead SOIC package.





(Top View)



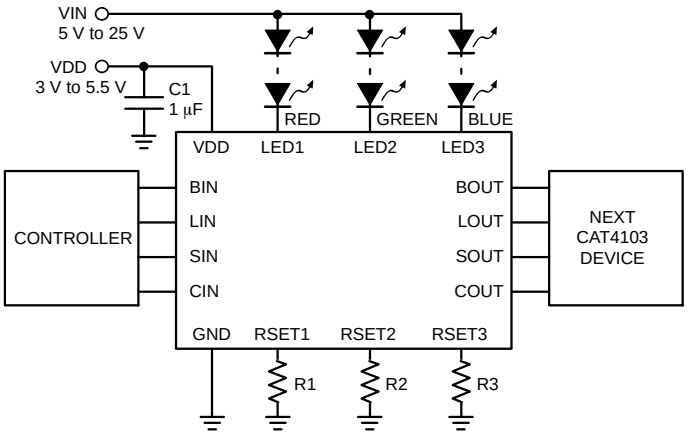
- 3 Independent Current Sinks Rated to 25 V
- LED Current to 175 mA per Channel Set by Separate External Resistors
- High speed 25 MHz 4 wire Serial Interface
- Buffered Output Drivers to Ensure Data Integrity
- Cascadable Devices
- Low Dropout Current Source (0.4 V at 175 mA)
- 3 V to 5.5 V Logic Supply
- Thermal Shutdown Protection
- 16 lead SOIC Package
- These Devices are Pb Free, Halogen Free/BFR Free and are RoHS Compliant

- Multi color, Intelligent LED, Architectural Lighting
- High visual Impact LED Signs and Displays
- LCD Backlight

CAT4103V−GT2 (Note 1)	SOIC−16 (Pb−Free)	2,000/ Tape & Reel

1. Lead Finish NiPdAu

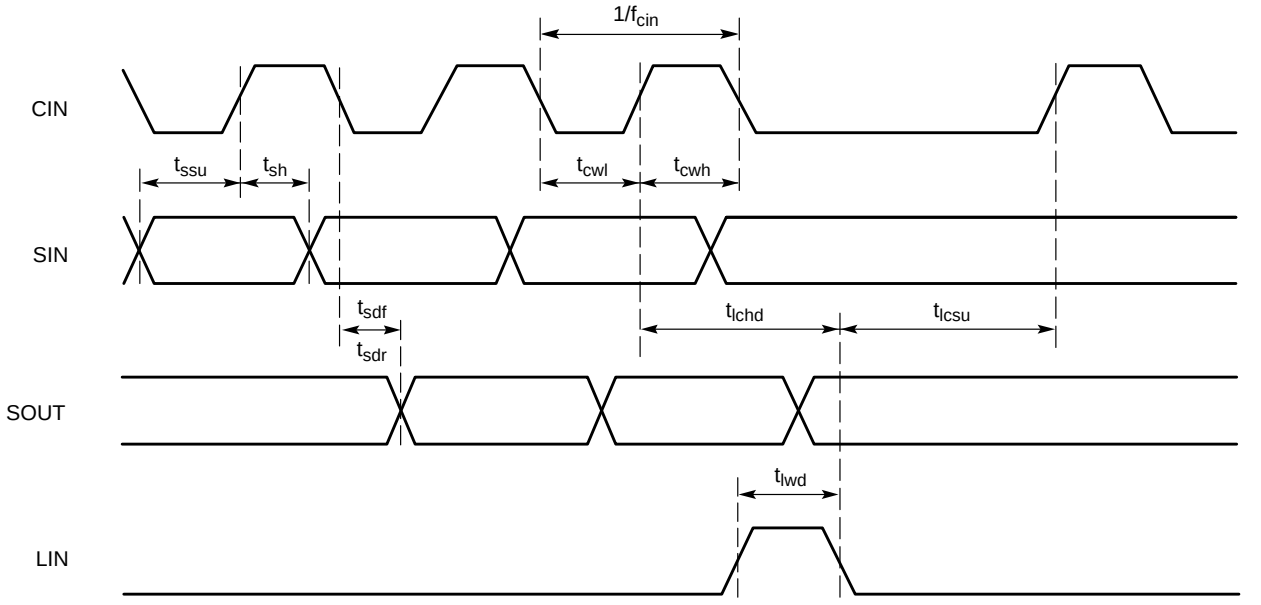
Publication Order Number:

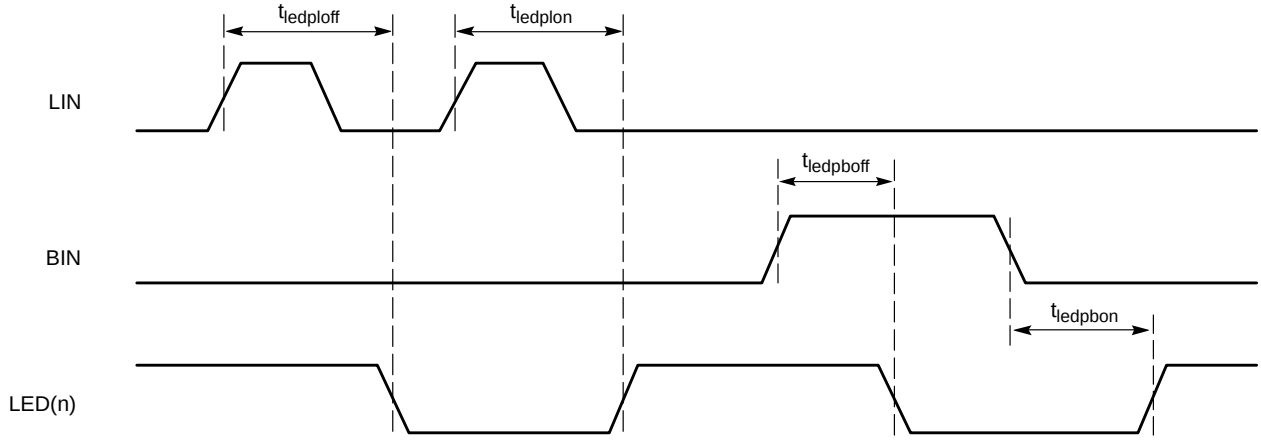


VDD Voltage	6	V
Input Voltage Range (SIN, BIN, CIN, LIN)	−0.3 V to VDD+0.3 V	V
Output voltage range (SOUT, BOUT, COUT, LOUT)	−0.3 V to VDD+0.3 V	V
LED1, LED2, LED3 Voltage	25	V
DC Output Current on LED1 to LED3		

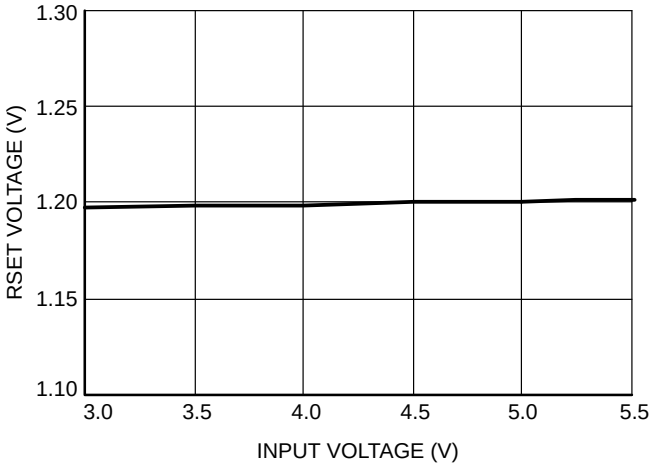
(Min and Max values are over recommended operating conditions unless specified otherwise. Typical values are at V_{IN} = 5.0 V, T_{AMB} = 25°C.)

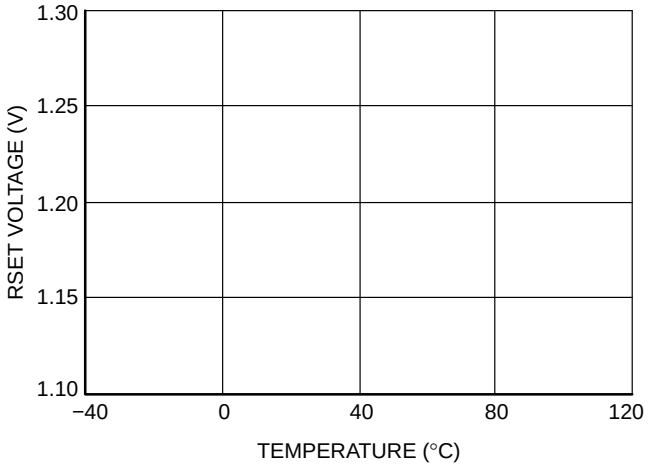
f_{cin}	CIN Clock Frequency				25	MHz
t_{cwh}	CIN Pulse Width High		18			ns
t_{cwl}	CIN Pulse Width Low		18			ns
t_{ssu}	Setup time SIN to CIN		4			ns
t_{sh}	Hold time SIN to CIN		4			ns
T_{lwh}	LIN Pulse width		20			ns
t_{lchd}	Hold time LIN to CIN		4			ns
t_{lcsu}	Setup time LIN to CIN		8			ns
$t_{ledplon}$	Turn on Propagation delay LIN	LIN to LED(n) on		380		ns
$t_{ledploff}$	Turn off Propagation delay LIN	LIN to LED(n) off		130		ns

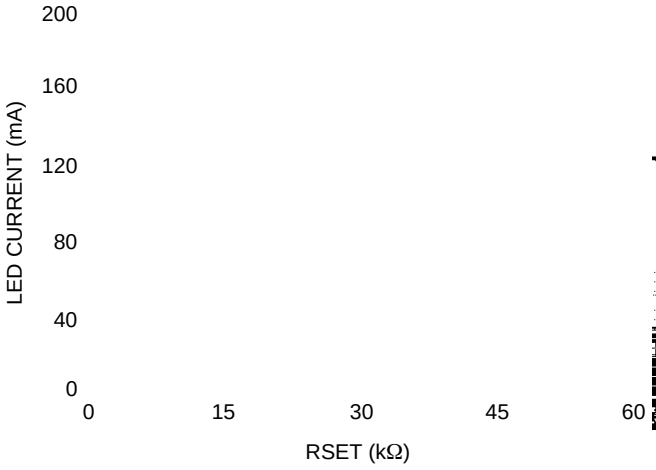

1/fcin
CIN
tssu
tsh
tcwl
tcwh
SIN
tsdf
tsdr
tlchd
tlcsu
SOUT
tlwd
LIN

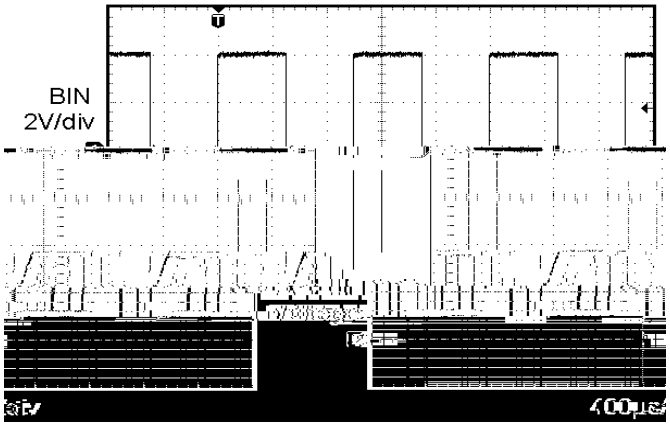

tledploff
tledplon
LIN
tledpboff
BIN
tledpbon
LED(n)

(V_{IN} = 5 V, V_{DD} = 5 V, C_1 = 1 μF, T_{AMB} = 25°C unless otherwise specified.)









GND	1	Ground Reference
BIN	2	Blank input pin
LIN	3	Latch Data input pin
SIN	4	Serial Data input pin
CIN	5	Serial Clock input pin
RSET3	6	LED current set pin for LED3
RSET2	7	LED current set pin for LED2
RSET1	8	LED current set pin for LED1
LED3	9	LED channel 3 cathode terminal
LED2	10	LED channel 2 cathode terminal
LED1	11	LED channel 1 cathode terminal
COUT	12	Serial Clock output pin
SOUT	13	Serial Data output pin
LOUT	14	Latch Data output pin
BOUT	15	Blank output pin
VDD	16	Device Supply pin

GND is the ground reference pin for the entire device. This pin must be connected to the ground plane on the PCB.

BIN is the blank input used to disable all channels. When low, all LED channels are enabled according to the output latch content. When high, all LED channels are turned off. This pin can be used to turn all the LEDs off while preserving the data in the output latches.

LIN is the latch data input. On the rising edge of LIN, data is loaded from the 3 bit serial shift register into the output register latch. On the falling edge of LIN the data is latched in the output register and isolated from the state of the serial shift register.

SIN is the serial data input. Data is loaded into the internal register on each rising edge of CIN.

CIN is the serial clock input. On each rising CIN edge, data is transferred from SIN to the internal 3 bit serial shift register.

RSET1 to RSET3 are the LED current set inputs. The current pulled out of these pins will be mirrored in the corresponding LED channel with a gain of 400.

LED1 to LED3 are the LED current sink inputs. These pins are connected to the bottom cathodes of the LED strings. The current sinks bias the LEDs with a current equal to 400 times the RSET pin current. For the LED sink to operate correctly, the voltage on the LED pin must be above 0.4 V. Each LED channel can withstand and operate with voltages up to 25 V.

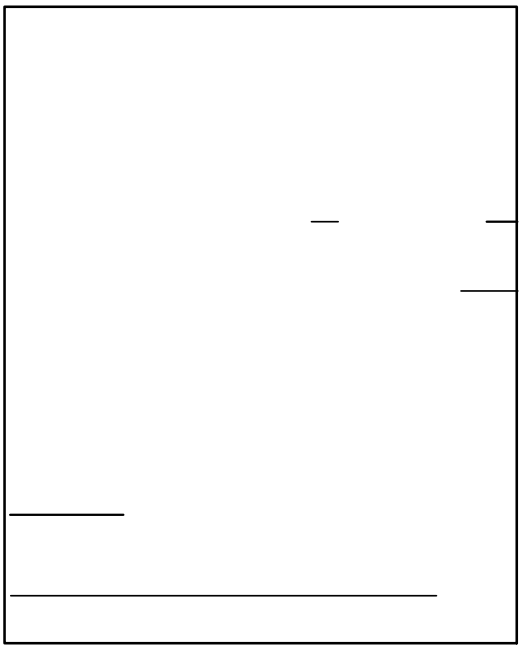
COUT is a driven output of CIN and can be connected to the next device in the cascade.

SOUT is the output of the 3 bit serial shift register. Connect to SIN of the next device in the cascade. SOUT is clocked on the falling edge of CIN.

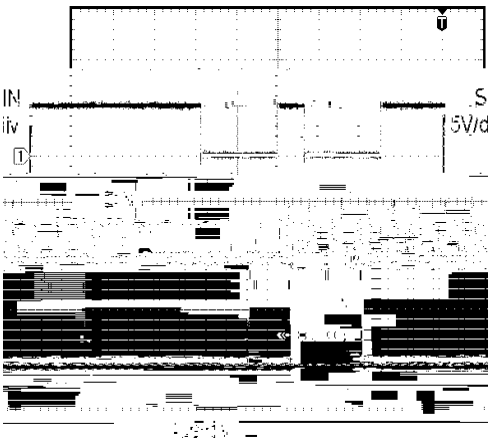
LOUT is a driven output of LIN and can be connected to the next chip in the cascade.

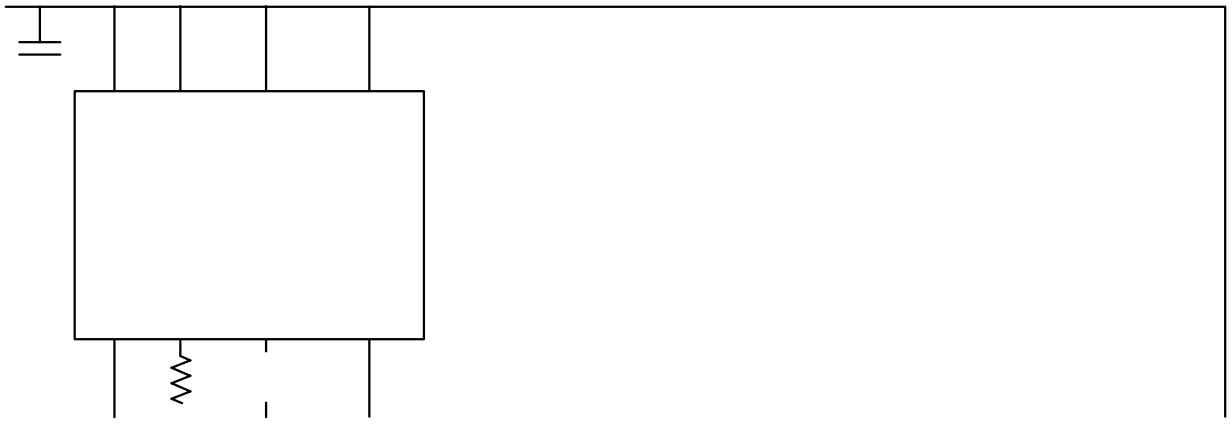
BOUT is a driven output of BIN and can be connected to the next chip in the cascade.

VDD is the positive supply pin voltage for the entire device. A small 1 μF ceramic capacitor is recommended close to the pin.



The CAT4103 is designed to be cascaded for driving multiple RGD LEDs. Figure 16 shows three CAT4103 drivers cascaded together. The programming data from the controller travels serially through each device. Figure 15 shows a programming example turning on the following LED channels: BLUE3, GREEN2 and RED1. The programming waveforms are measured from the controller to the inputs of the first CAT4103.





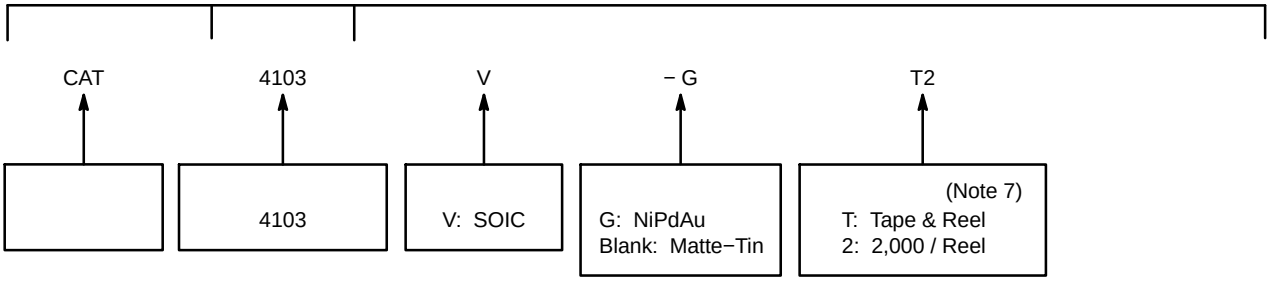
The power dissipation (P_D) of the CAT4103 can be calculated as follows:

$$P_D = (V_{DD} \times I_{DD}) + \Sigma(V_{LEDN} \times I_{LEDN})$$

where V_{LEDN} is the voltage at the LED pin, and I_{LEDN} is the associated LED current. Combinations of high V_{LED} voltage or high ambient temperature can cause the CAT4103 to enter thermal shutdown. In applications where V_{LEDN} is high, a resistor can be inserted in series with the LED string to lower P_D.

Thermal dissipation of the junction heat consists primarily of two paths in series. The first path is the junction to the case (θ_{JC}) thermal resistance which is defined by the package style, and the second path is the case to ambient

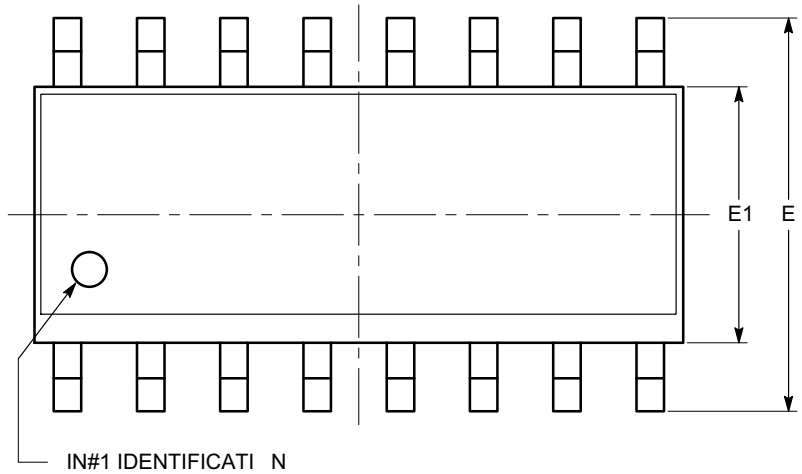
(Note 5)



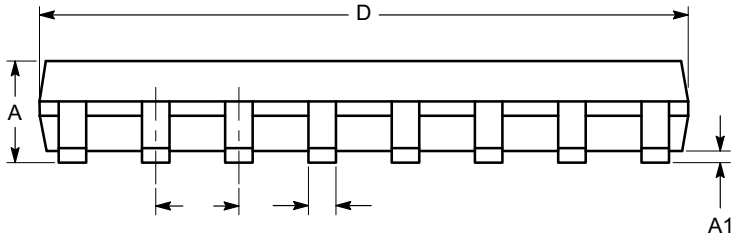
3. All packages are RoHS−compliant (Lead−free, Halogen−free).
4. The standard plated finish is NiPdAu.
5. The device used in the above example is a CAT4103V−GT2 (SOIC, NiPdAu, Tape & Reel, 2,000/Reel).
6. For additional temperature options, please contact your nearest ON Semiconductor Sales office.
7. For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

SOIC−16, 150 mils
CASE 751BG−01
ISSUE O

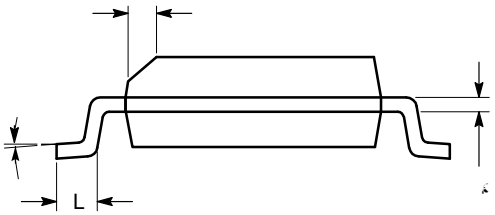
DATE 19 DEC 2008



TOP VIEW



SIDE VIEW



END VIEW

Notes:
(1) A [illegible] n [illegible] na [illegible] n m [illegible] m [illegible] . An [illegible] n [illegible] .
(2) C [illegible] JEDEC MS-012.

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