



($V_{DD} = 5.0\text{ V}$, $T_{AMB} = 25^{\circ}\text{C}$, over recommended operating conditions unless specified otherwise.)

$I_{LED-ACC}$	LED Current (any channel)	$V_{LED} = 1\text{ V}$, $R_{SET} = 3.08\text{ k}\Omega$	18	20	22	mA
		$V_{LED} = 1\text{ V}$, $R_{SET} = 1.54\text{ k}\Omega$	36	40	44	
		$V_{LED} = 1\text{ V}$, $R_{SET} = 769\ \Omega$		80		
$I_{LED-MAT}$	LED Current Matching $(I_{LED} - I_{LEDAVR}) / I_{LEDAVR}$	$V_{LED} = 1\text{ V}$, $R_{SET} = 3.08\text{ k}\Omega$		± 1.5		%
		$V_{LED} = 1\text{ V}$, $R_{SET} = 1.54\text{ k}\Omega$	-6.0	± 1.5	+6.0	
		$V_{LED} = 1\text{ V}$, $R_{SET} = 769\ \Omega$		± 2.0		
ΔI_{VDD}	LED current regulation vs. V_{DD}	V_{DD} within 4.5 V and 5.5 V LED current 30 mA		± 0.1		% / V
ΔI_{VLED}	LED current regulation vs. V_{LED}	V_{LED} within 1 V and 3 V LED current 30 mA		± 0.05		% / V
I_{DDOFF}						

(For $3.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $T_{AMB} = 25^\circ\text{C}$, unless specified otherwise.)

			(Note 1)	(Note 2)	(Note 1)	
--	--	--	----------	----------	----------	--

f_{clk}	CLK Clock Frequency				25	MHz
t_{cwh}	CLK Pulse Width High		20			ns
t_{cwl}	CLK Pulse Width Low		20			ns

t_{ssu}	Setup time SIN to CLK		4			ns
t_{sh}	Hold time SIN to CLK		4			ns

t_{lwh}	LATCH Pulse width		20			ns
T_{lh}	Hold time LATCH to CLK		4			ns
T_{lsu}	Setup time LATCH to CLK	Channel Stagger Delay	400			ns

t_{ld}	LED1 Propagation delay	LATCH to LED1 off/on		40	300	ns
t_{ls}	LED Propagation delay stagger	LED(n) to LED(n+1)		17	40	ns
t_{lst}	LED Propagation delay stagger total	LED1 to LED8		120		ns
t_{bd}	BLANK Propagation delay	BLANK to LED(n) off/on		60	300	ns
t_{lr}	LED rise time (10% to 90%)	Pull-up resistor = $50\ \Omega$ to 3.0 V		40	200	ns
t_{lf}	LED fall time (90% to 10%)	Pull-up resistor = $50\ \Omega$ to 3.0 V		30	250	ns

t_{or}	SOUT rise time (10% to 90%)	$C_L = 15\text{ pF}$		5		ns
t_{of}	SOUT fall time (90% to 10%)	$C_L = 15\text{ pF}$		5		ns
t_{od}	Propagation delay time SOUT	CLK to SOUT	8	15	25	ns

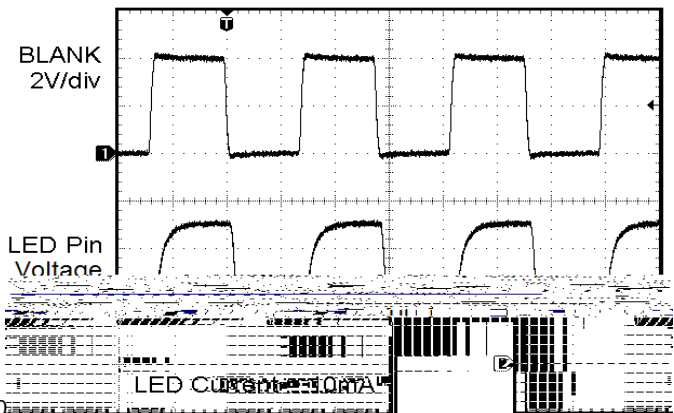
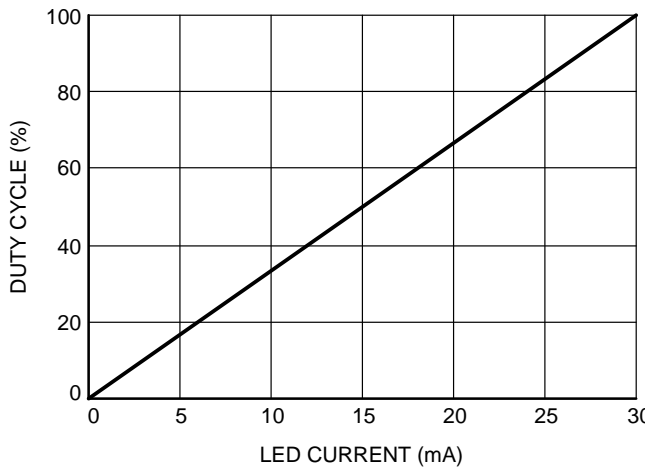
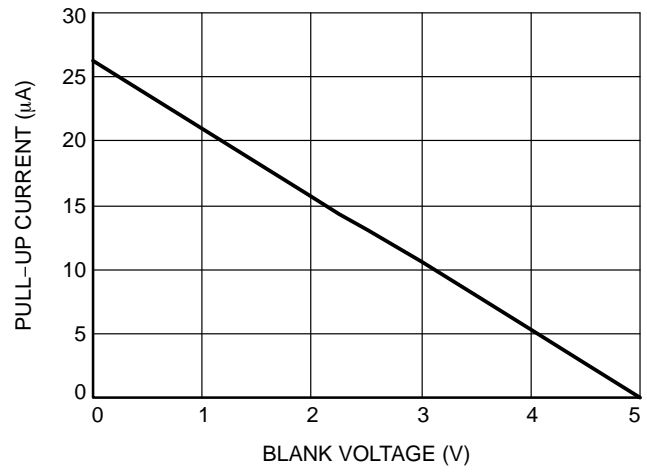
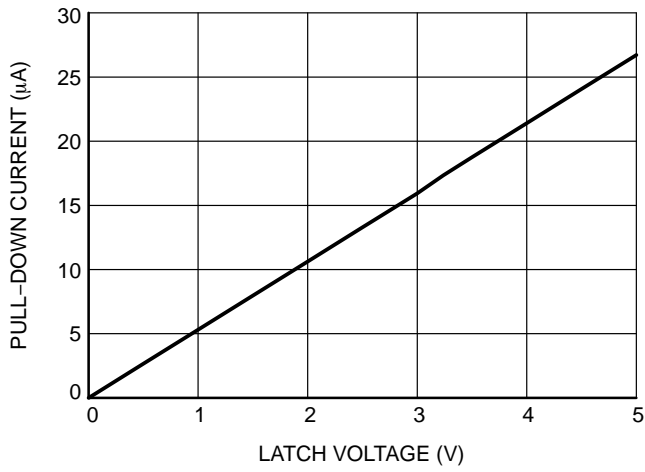
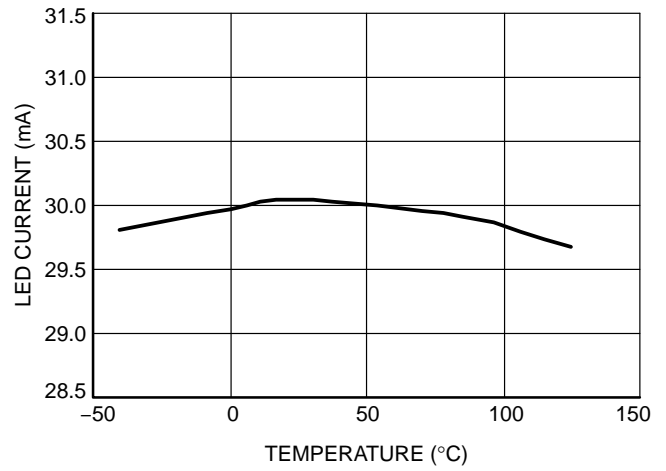
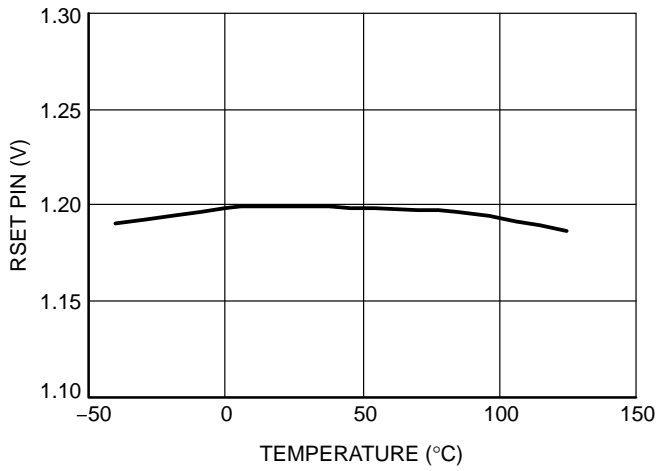
1. All min and max values are guaranteed by design.
2. $V_{DD} = 5\text{ V}$, LED current 30 mA.

—
|

|



($V_{DD} = 5.0\text{ V}$, LED CURRENT 30 MA, ALL LEDS ON, $T_{AMB} = 25^\circ\text{C}$ UNLESS OTHERWISE SPECIFIED.)



GND	Ground
SIN	Serial data input pin
CLK	Serial clock input pin
LATCH	Latch serial data to output registers
LED1-LED8	LED channel 1 to 8 cathode terminals
BLANK	Enable / disable all channels
SOUT	Serial data output pin.
RSET	LED current set pin
VDD	Positive supply Voltage

GND

BLANK

SIN

CLK

SOUT

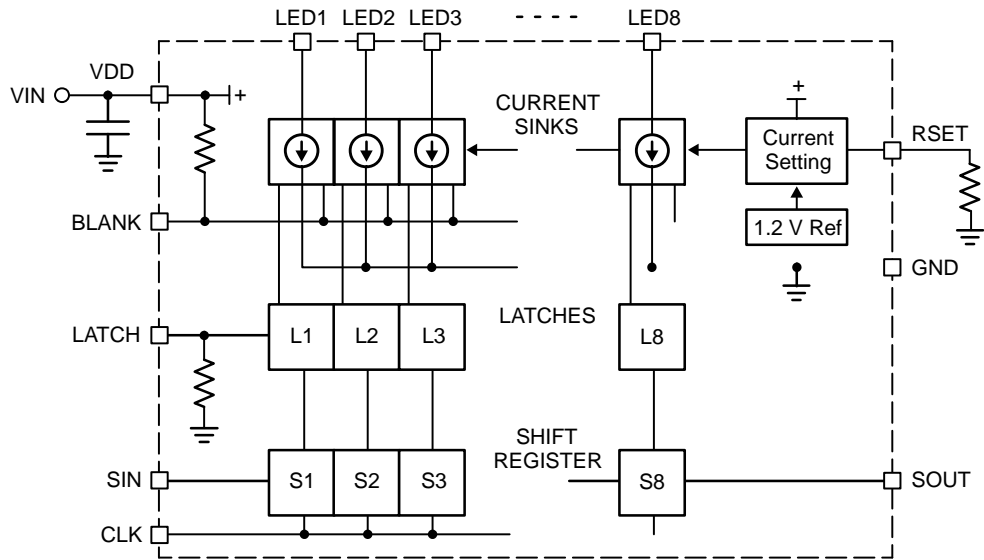
LATCH

RSET

LED1 – LED8

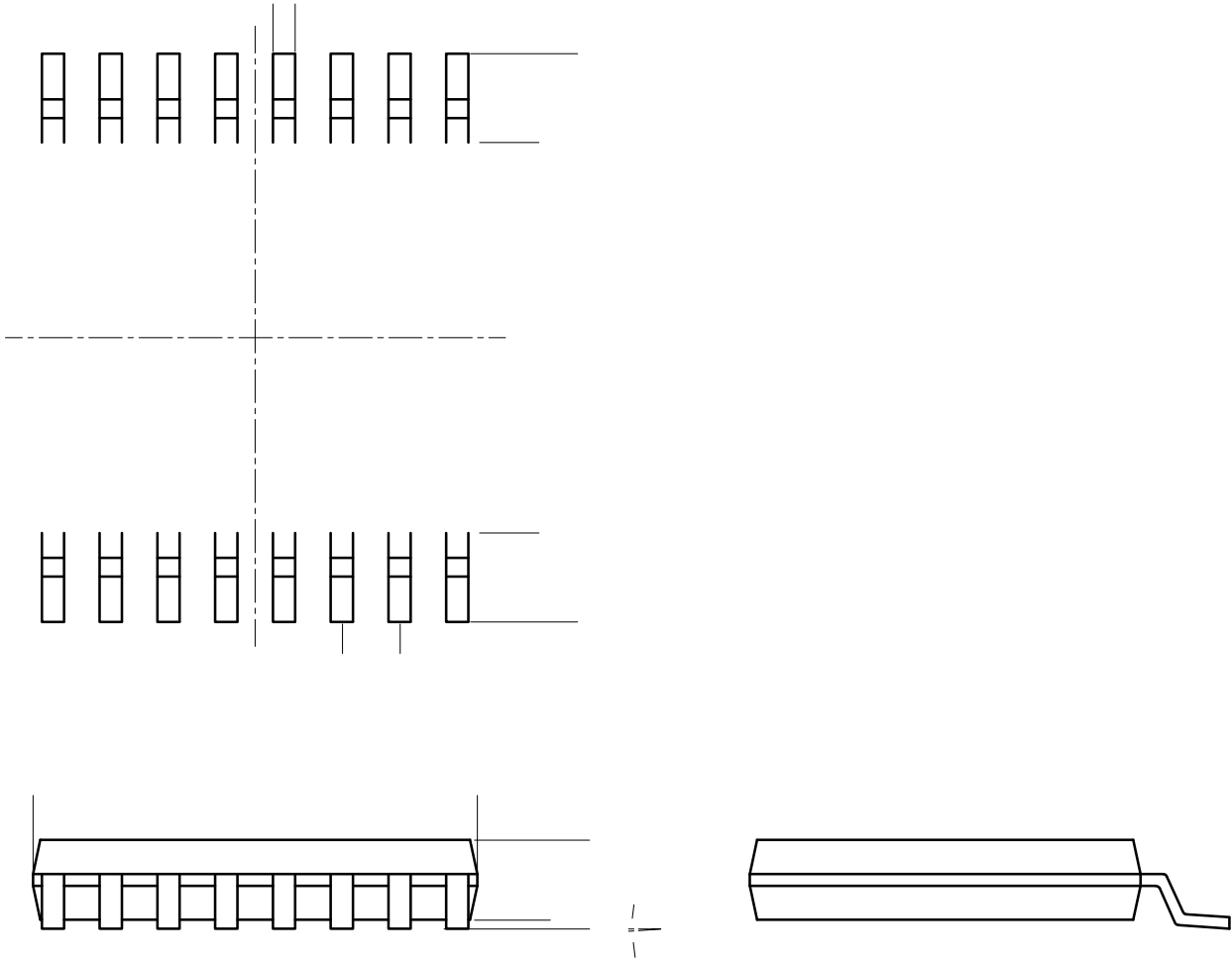
VDD

μ



TSSOP16, 4.4x5
CASE 948AN
ISSUE O

DATE 19 DEC 2008



onsemi, **onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi**
