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Description

CAT34TS00 is a low-voltage digital temperature sensor, which implements the JEDEC JC42.4 specification. CAT34TS00 measures temperature every 100 ms over a range of −20°C to +125°C, with a resolution of 12 bits.

The host communicates with the device via the serial I^2C / SMBus Interface, at either 100 kHz or 400 kHz. Temperature readings can be retrieved via serial interface. Internally, they are compared to high, low and critical trigger limits stored in device registers. Over or under limit conditions can be signaled on the open−drain EVENT pin. These limits, as well as other settings, can be configured via serial interface.

Features

- JEDEC JC42.4 Compliant Temperature Sensor
- Supply Range: 1.7 V to 1.9 V
- Temperature Range: −20°C to +125°C
- I^2C / SMBus Interface
- Temperature Sampling Rate: 100 ms max
- Temperature Reading Accuracy:
  ±0.5°C typ for Active Range (+75°C to +95°C)
- Schmitt Triggers and Noise Suppression Filters on SCL and SDA Inputs
- 2 x 3 x 0.75 mm TDFN Package
- These Devices are Pb−Free and are RoHS Compliant

Typical Applications

- Solid State Drives
- Graphics Cards
- Portable Devices
- Process Control Equipment

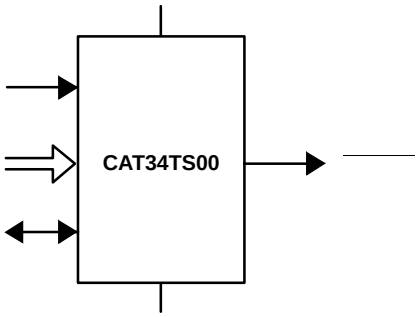


Figure 1. Functional Symbol

Table 1. ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Unit
	–	
	–	
	–	°
	–	°

–

–

Table 2. TEMPERATURE CHARACTERISTICS

Parameter	Conditions	Typ	Max	Unit
	° ≤ ≤ °	±	±	°
	° ≤ ≤ °	±	±	°
	– ° ≤ ≤ °	±	±	°
				°
θ	– –			°

– θ

–

Table 3. D.C. OPERATING CHARACTERISTICS – ° °

Symbol	Parameter	Test Conditions/Comments	Min	Max	Unit
					µ
		–			µ
					µ
			–		

Table 4. A.C. CHARACTERISTICS – ° °

Symbol	Parameter	100 kHz		400 kHz		Units
		Min	Max	Min	Max	
						µ
						µ

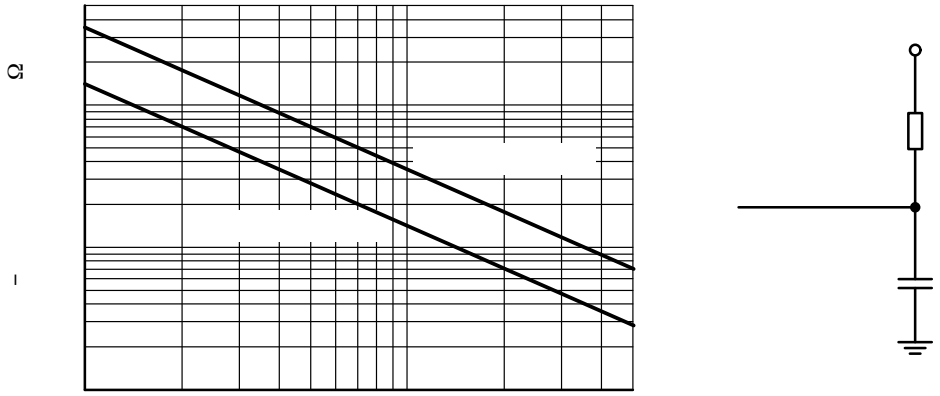


Figure 2. Pull−up Resistance vs. Load Capacitance

Pin Description

SCL: The Serial Clock input pin accepts the Serial Clock generated by the Master (Host).

SDA: The Serial Data I/O pin receives input data and transmits data stored in the TS registers. In transmit mode, this pin is open drain. Data is acquired on the positive edge, and is delivered on the negative edge of SCL.

A0, A1 and A2: The Address pins accept the device address. These pins have on−chip pull−down resistors.

$\overline{\text{EVENT}}$: The open−drain $\overline{\text{EVENT}}$ pin can be programmed to signal over/under temperature limit conditions.

Power−On Reset (POR)

The CAT34TS00 incorporates Power−On Reset (POR) circuitry which protects the device against powering up to an undetermined logic state. As V_{CC} exceeds the POR trigger level, the device will power up into conversion mode. When V_{CC} drops below the POR trigger level, the device will power down into Reset mode.

This bi−directional POR behavior protects CAT34TS00 against brown−out failure following a temporary loss of power. The POR trigger level is set below the minimum operating V_{CC} level.

Device Interface

The CAT34TS00 supports the Inter−Integrated Circuit (I^2C) and the System Management Bus (SMBus) data transmission protocols. These protocols describe serial communication between transmitters and receivers sharing a 2−wire data bus. Data flow is controlled by a Master device,

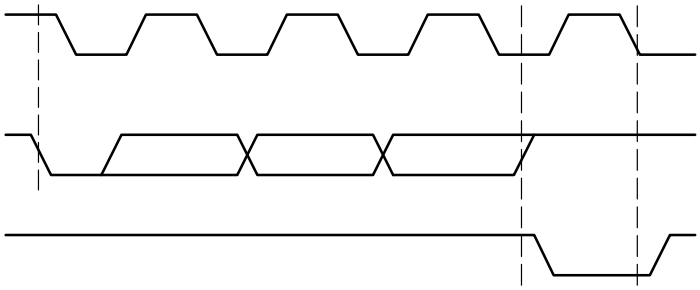
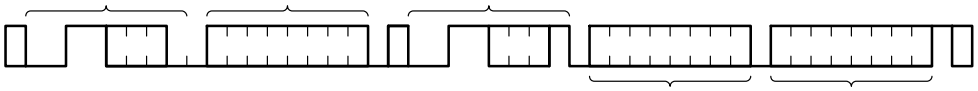


Figure 4. Acknowledge Timing



Manufacturer ID Register (Read Only)

The manufacturer ID assigned by the PCI−SIG trade organization to the CAT34TS00 device is fixed at 0x1B09.

Device ID and Revision Register (Read Only)

This register contains specific device ID and device revision information.

Table 7. THE TEMPERATURE SENSOR REGISTERS

Register Address	Register Name	Power−On Default	Read/Write

Table 9. CONFIGURATION REGISTER

B15	B14	B13	B12	B11	B10	B9	B8
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**

Bit	Description
B15:B11	
B10:B9	◦ ◦ ◦
B8	
B7	
B6	

Table 10. HIGH LIMIT REGISTER

B15	B14	B13	B12	B11	B10	B9	B8
				◦	◦	◦	◦
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
◦	◦	◦	◦				

Register Data Format

The values used in the temperature data register and the 3 temperature trip point registers are expressed in two's complement format. The measured temperature value is expressed with 12−bit resolution, while the 3 trip temperature limits are set with 10−bit resolution. The total temperature range is arbitrarily defined as 256°C, thus yielding an LSB of 0.0625°C for the measured temperature and 0.25°C for the 3 limit values. Bit B12 in all temperature registers represents the sign, with a '0' indicating a positive, and a '1' a negative value. In two's complement format, negative values are obtained by complementing their positive counterpart and adding a '1', so that the sum of opposite signed numbers, but of equal absolute value, adds up to zero.

Note that trailing '0' bits, are '0' irrespective of polarity. Therefore the "don't care" bits (B1 and B0) in the 10−bit resolution temperature limit registers, are always '0'.

Table 14. 12−BIT TEMPERATURE DATA FORMAT

Binary (B12 to B0)	Hex	Temperature
		– °
		– °
		– °
		– °
		°
		°
		°
		°
		°

Event Pin Functionality

The $\overline{\text{EVENT}}$ output reacts to temperature changes as illustrated in Figure 9, and according to the operating mode defined by the Configuration register.

In **Interrupt Mode**, the (enabled) $\overline{\text{EVENT}}$ output will be asserted every time the temperature crosses one of the alarm window limits, and can be de−asserted by writing a '1' to the clear event bit (B5) in the configuration register. Once the temperature exceeds the critical limit, the $\overline{\text{EVENT}}$ remains asserted as long as the temperature stays above the critical limit and cannot be cleared. A clear request sent to the CAT34TS00 while the temperature is above the critical limit will be acknowledged, but will be executed only after the temperature drops below the critical limit.

In **Comparator Mode**, the $\overline{\text{EVENT}}$ output is asserted outside the alarm window limits, while in **Critical Temperature Mode**, $\overline{\text{EVENT}}$ is asserted only above the critical limit. Clear requests are ignored in this mode. The exact trip limits are determined by the 3 temperature limit settings and the hysteresis offsets, as illustrated in Figure 10.

Following a TS shut−down request, the converter is stopped and the most recently recorded temperature value present in the TDR is frozen; the $\overline{\text{EVENT}}$ output will continue to reflect the state immediately preceding the shut−down command. Therefore, if the state of the $\overline{\text{EVENT}}$ output creates an undesirable bus condition, appropriate action must be taken either before or after shutting down the TS. This may require clearing the event, disabling the $\overline{\text{EVENT}}$ output or perhaps changing the $\overline{\text{EVENT}}$ output polarity.

In normal use, events are triggered by a change in recorded temperature, but the CAT34TS00 will also respond to limit register changes. Whereas recorded temperature values are updated at sampling rate frequency, limits can be modified at any time. The enabled $\overline{\text{EVENT}}$ output will react to limit changes as soon as the respective registers are updated. This feature may be useful during testing.

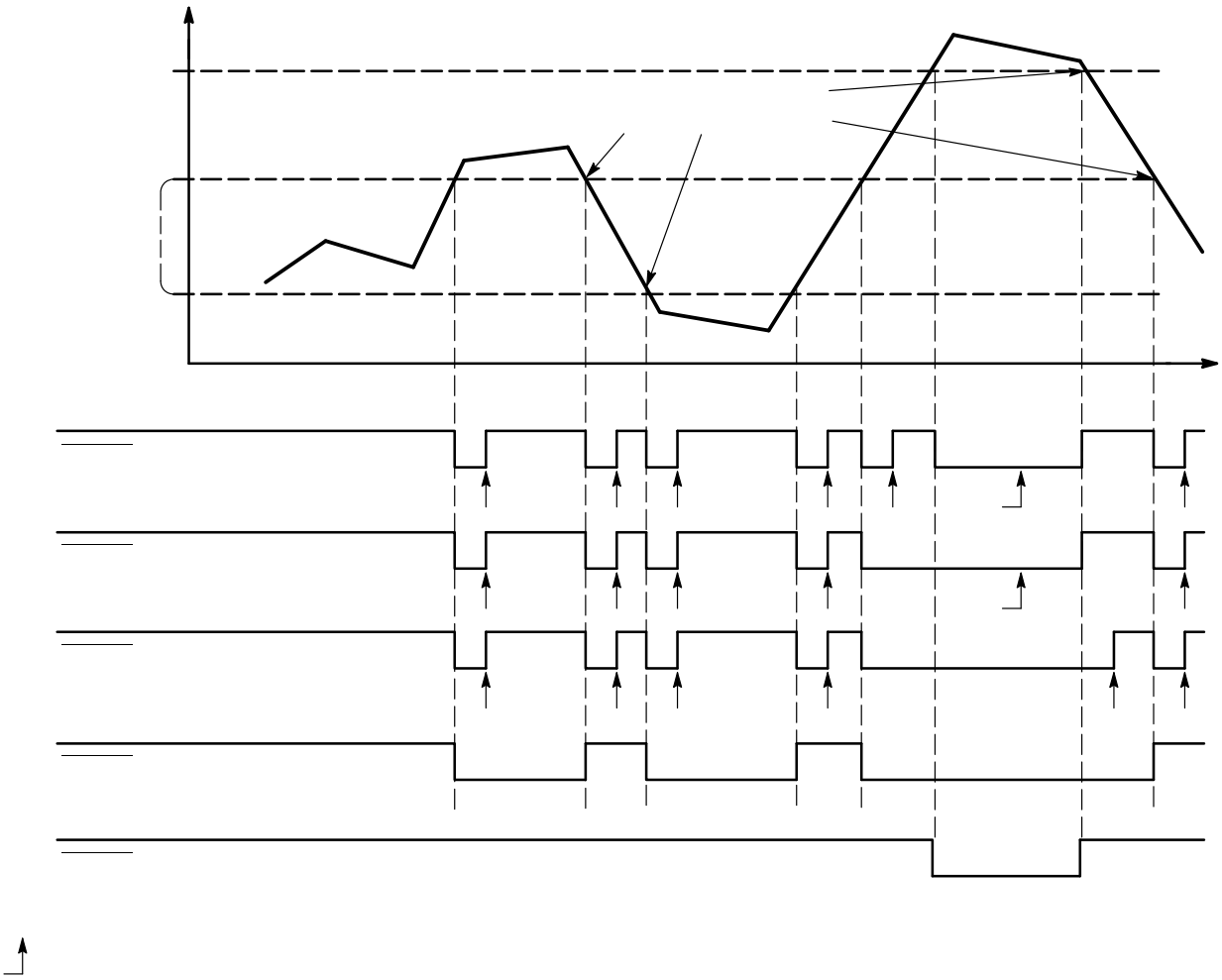


Figure 9. Event Detail

Example of Ordering Information

Device Order Number	Specific Device Marking	Package Type	Shipping

TDFN8, 2x3, 0.5P
CASE 511AK
ISSUE B

SCALE 2:1

DATE 18 MAR 2015

NOTES: