



# CAT24C512C8UTR

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## EEPROM Serial 512-Kb I<sup>2</sup>C

### Description

The CAT24C512 is a EEPROM Serial 512-Kb I<sup>2</sup>C internally organized as 65,536 words of 8 bits each.

It features a 128-byte page write buffer and supports the Standard (100 kHz), Fast (400 kHz) and Fast-Plus (1 MHz) I<sup>2</sup>C protocol.

Write operations can be inhibited by taking the WP pin High (this protects the entire memory).

External address pins make it possible to address up to eight CAT24C512 devices on the same bus.

On-Chip ECC (Error Correction Code) makes the device suitable for high reliability applications.

### Features

Supports Standard, Fast and Fast-Plus I<sup>2</sup>C Protocol

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**Table 1. ABSOLUTE MAXIMUM RATINGS**

| Parameters                                         | Ratings      | Units |
|----------------------------------------------------|--------------|-------|
| Storage Temperature                                | -65 to +150  | C     |
| Voltage on any Pin with Respect to Ground (Note 1) | -0.5 to +6.5 | V     |

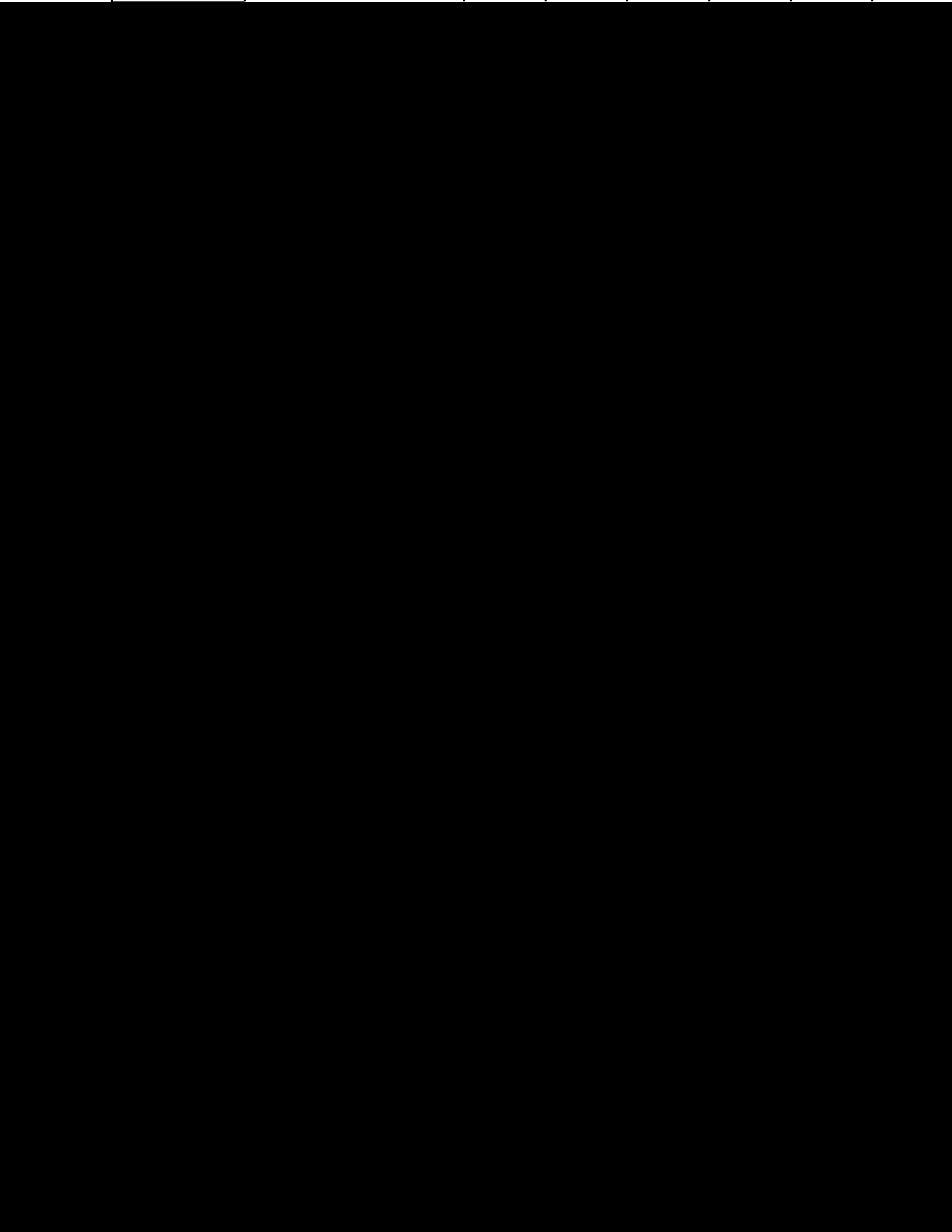
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

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**Table 5. A.C. CHARACTERISTICS** (Note 7)

$V_{CC} = 1.8\text{ V to }5.5\text{ V}$ ,  $T_A = -40\text{ C to }+85\text{ C}$  and  $V_{CC} = 2.5\text{ V to }5.5\text{ V}$ ,  $T_A = -40\text{ C to }+125\text{ C}$ , unless otherwise specified.

| Symbol | Parameter | Standard<br>$V_{CC} = 1.8\text{ V} - 5.5\text{ V}$ |     | Fast<br>$V_{CC} = 1.8\text{ V} - 5.5\text{ V}$ |     | Fast-Plus<br>$V_{CC} = 2.5\text{ V} - 5.5\text{ V}$<br>$T_A = -40\text{ C to }+85\text{ C}$ |     | Units |
|--------|-----------|----------------------------------------------------|-----|------------------------------------------------|-----|---------------------------------------------------------------------------------------------|-----|-------|
|        |           | Min                                                | Max | Min                                            | Max | Min                                                                                         | Max |       |



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## Power-On Reset (POR)

The CAT24C512 incorporates Power-On Reset (POR) circuitry which protects the internal logic against powering up in the wrong state.

The device will power up into Standby mode after  $V_{CC}$  exceeds the POR trigger level and will power down into Reset mode when  $V_{CC}$  drops below the POR trigger level.

*This bi-directional POR behavior protects the device against brown-out failure, following a temporary loss of power.*

## Pin Description

**SCL:** The Serial Clock input pin accepts the Serial Clock signal generated by the Master.

**SDA:** The Serial Data I/O pin receives input data and transmits data stored in EEPROM. In transmit mode, this pin is open drain. Data is acquired on the positive edge, and is delivered on the negative edge of SCL.

**A<sub>0</sub>, A<sub>1</sub> and A<sub>2</sub>:** The Address pins accept the device address. These pins have on-chip pull-down resistors.

**WP:** The Write Protect input pin inhibits all write operations, when pulled HIGH. This pin has an on-chip pull-down resistor.

## Functional Description

The CAT24C512 supports the Inter-Integrated Circuit (I<sup>2</sup>C) Bus data transmission protocol, which defines a device that sends data to the bus as a transmitter and a device receiving data as a receiver. Data flow is controlled by a Master device, which generates the serial clock and all START and STOP conditions. The CAT24C512 acts as a Slave device. Master and Slave alternate as either transmitter or receiver. Up to 8 devices may be connected to the bus as determined by the device address inputs A<sub>0</sub>, A<sub>1</sub>, and A<sub>2</sub>.

## I<sup>2</sup>C Bus Protocol

The I<sup>2</sup>C bus consists of two 'wires', SCL and SDA. The two wires are connected to the  $V_{CC}$  supply via pull-up resistors. Master and Slave devices connect to the 2-wire bus via their respective SCL and SDA pins. The transmitting

device pulls down the SDA line to 'transmit' a '0' and releases it to 'transmit' a '1'.

Data transfer may be initiated only when the bus is not busy (see A.C. Characteristics).

During data transfer, the SDA line must remain stable while the SCL line is HIGH. An SDA transition while SCL is HIGH will be interpreted as a START or STOP condition (Figure 2).

## START

The STpul8.1(p-.043j9te4001 Tc0 Tw(((Figu7gf9 omm2 TingIt 'wires', S

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START

## WRITE OPERATIONS

### Byte Write

In Byte Write mode the Master sends a START, followed by Slave address, two byte address and data to be written (Figure 6). The Slave acknowledges all 4 bytes, and the Master then follows up with a STOP, which in turn starts the internal Write operation (Figure 7). During internal Write, the Slave will not acknowledge any Read or Write request from the Master.

### Page Write

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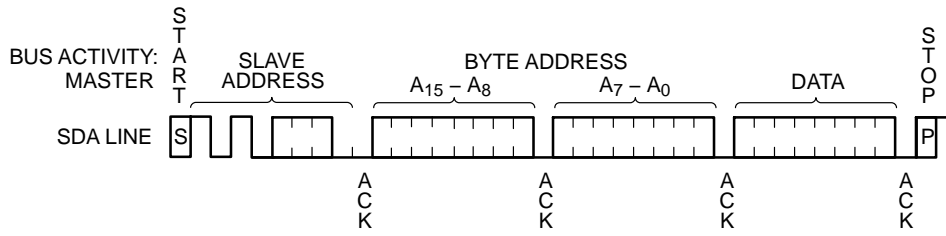


Figure 6. Byte Write Timing

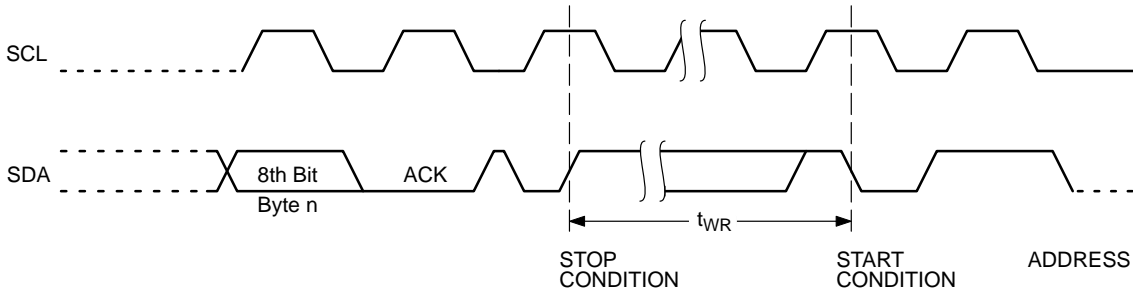


Figure 7. Write Cycle Timing

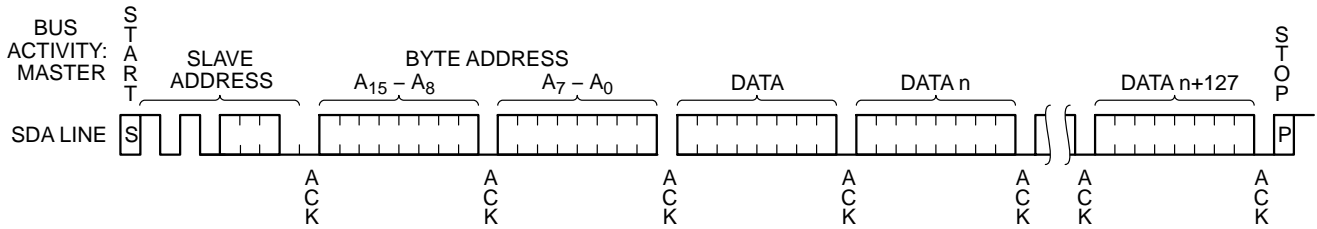


Figure 8. Page Write Timing

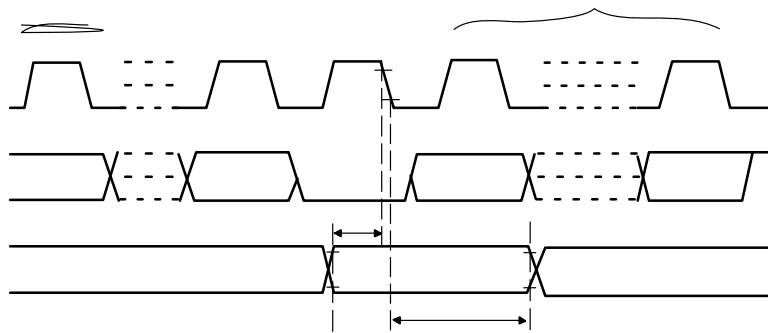


Figure 9. WP Timing



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## READ OPERATIONS

### Immediate Address Read

In standby mode, the CAT24C512 internal address counter points to the data byte immediately following the last byte accessed by a previous operation. If that 'previous' byte was the last byte in memory, then the address counter will point to the 1st memory byte, etc.

When, following a START, the CAT24C512 is presented with a Slave address containing a '1' in the R/W bit position (Figure 10), it will acknowledge (ACK) in the 9th clock cycle, and will then transmit data being pointed at by the internal address counter. The Master can stop further transmission by issuing a NoACK, followed by a STOP condition.

### Selective Read

The Read operation can also be started at an address different from the one stored in the internal address counter.

The address counter can be initialized by performing a 'dummy' Write operation (Figure 11). Here the START is followed by the Slave address (with the R/W bit set to '0') and the desired two byte address. Instead of following up with data, the Master then issues a 2nd START, followed by the 'Immediate Address Read' sequence, as described earlier.

### Sequential Read

If the Master acknowledges the 1st data byte transmitted by the CAT24C512, then the device will continue transmitting as long as each data byte is acknowledged by the Master (Figure 12). If the end of memory is reached during sequential Read, then the address counter will 'wrap-around' to the beginning of memory, etc. Sequential Read works with either 'Immediate Address Read' or 'Selective Read', the only difference being the starting byte address.

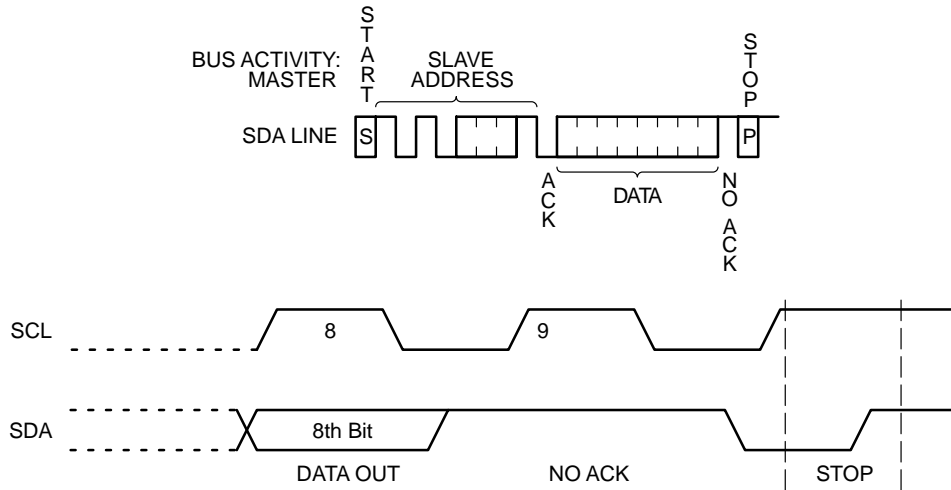


Figure 10. Immediate Address Read Timing

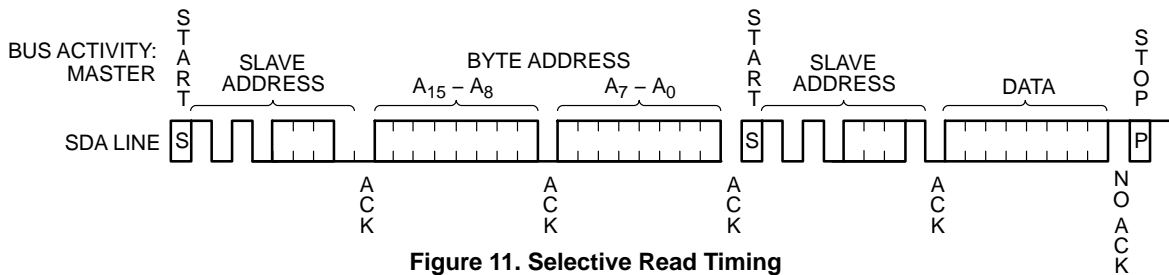


Figure 11. Selective Read Timing

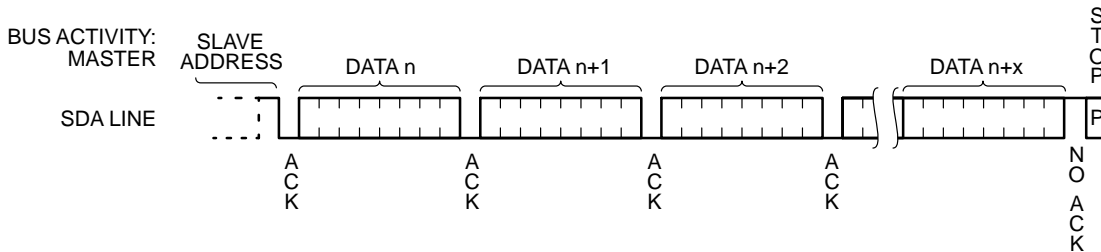


Figure 12. Sequential Read Timing

ORDERING INFORMATION

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## PACKAGE DIMENSIONS

WLCSP8 1.39x1.65x0.40  
CASE 567WK  
ISSUE B

BY THE SPHERICAL CR

| DIM | MILLIMETERS |      |      |
|-----|-------------|------|------|
|     | MIN.        | NDM. | MAX. |
| A   | ---         | ---  | 0.40 |
| A1  | 0.06        | 0.08 | 0.10 |
| A2  | 0.270 REF   |      |      |
| A3  | 0.025 REF   |      |      |
| b   | 0.22        | 0.24 | 0.26 |
| D   | 1.29        | 1.39 | 1.49 |
| E   | 1.55        | 1.65 | 1.75 |
| e   | 0.500 BSC   |      |      |
| e1  | 0.433 BSC   |      |      |

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