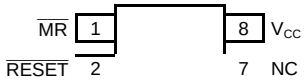
BLOCK DIAGRAM

THRESHOLD VOLTAGE OPTION

Part Dash Number	Minimum Threshold	Maximum Threshold
-45	4.50	4.75
-42	4.25	4.50
-30	3.00	3.15
-28	2.85	3.00
-25	2.55	2.70

PIN CONFIGURATION

DIP Package (L)
SOIC Package (W)
TSSOP Package (Y)
MSOP Package (Z)



PIN DESCRIPTION

RESET/$\overline{\text{RESET}}$: RESET OUTPUTs
(RESET CAT1025 Only)
These are open drain pins and $\overline{\text{RESET}}$ can be used as a manual reset trigger input. By forcing a reset condition on the pin the device will initiate and maintain a reset condition. The RESET pin must be connected through a pull-down resistor, and the $\overline{\text{RESET}}$ pin must be connected through a pull-up resistor.

SDA: SERIAL DATA ADDRESS
The bidirectional serial data/address pin is used to transfer all data into and out of the device. The SDA pin is an open drain output and can be wire-ORed with other open drain or open collector outputs.

SCL: SERIAL CLOCK
Serial clock input.

$\overline{\text{MR}}$: MANUAL RESET INPUT
Manual Reset input is a debounced input that can be connected to an external source for Manual Reset. Pulling the MR input low will generate a Reset condition. Reset outputs are active while $\overline{\text{MR}}$ input is low and for the reset timeout period after $\overline{\text{MR}}$ returns high. The input has an internal pull-up resistor.

ABSOLUTE MAXIMUM RATINGS[1]

Parameters	Ratings	Units
Temperature Under Bias	–55 to +125	°C

RESET CIRCUIT AC CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
t_{PURST}	Power-Up Reset Timeout	Note 2	130	200	270	ms
t_{RDP}	V_{TH} to RESET Output Delay	Note 3			5	µs
t_{GLITCH}	V_{CC} Glitch Reject Pulse Width	Note 4, 5			30	ns
MR Glitch	Manual Reset Glitch Immunity	Note 1			100	ns
t_{MRW}	MR Pulse Width	Note 1	5			µs
t_{MRD}	MR Input to RESET Output Delay	Note 1			1	µs

POWER-UP TIMING (5), (6)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
t_{PUR}	Power-Up to Read Operation				270	ms
t_{PUW}	Power-Up to Write Operation				270	ms

AC TEST CONDITIONS

Parameter	Test Conditions
Input Pulse Voltages	0.2 x V_{CC} to 0.8 x V_{CC}
Input Rise and Fall Times	10 ns
Input Reference Voltages	0.3 x V_{CC}, 0.7 x V_{CC}
Output Reference Voltages	0.5 x V_{CC}

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Reference Test Method	Min	Max	Units
N_{END} (5)	Endurance	MIL-STD-883, Test Method 1033	1,000,000		Cycles/Byte
T_{DR} (5)	Data Retention	MIL-STD-883, Test Method 1008	100		Years
V_{ZAP} (5)	ESD Susceptibility	MIL-STD-883, Test Method 3015	2000		Volts
I_{LTH} (5)(7)	Latch-Up	JEDEC Standard 17	100		mA

Notes:

(1) Test Conditions according to “AC Test Conditions” table.

(2) Power-up, Input Reference Voltage $V_{CC} = V_{TH}$, Reset Output Reference Voltage and Load according to “AC Test Conditions” Table

(3) Power-Down, Input Reference Voltage $V_{CC} = V_{TH}$, Reset Output Reference Voltage and Load according to “AC Test Conditions” Table

(4) V_{CC} Glitch Reference Voltage = V_{THmin}; Based on characterization data

(5) This parameter is characterized initially and after a design or process change that affects the parameter. Not 100% tested.

(6) t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified memory operation can be initiated.

(7) Latch-up protection is provided for stresses up to 100 mA on input and output pins from -1 V to V_{CC} + 1 V.

DEVICE OPERATION

Reset Controller Description

The CAT1024/25 precision RESET controllers ensure correct system operation during brownout and power up/down conditions. They are configured with open drain RESET outputs.

During power-up, the RESET outputs remain active until V_{CC} reaches the V_{TH} threshold and will continue driving the outputs for approximately 200 ms (t_{PURST}) after reaching V_{TH}. After the t_{PURST} timeout interval, the device will cease to drive the reset outputs. At this point the reset outputs will be pulled up or down by their respective pull up/down resistors.

During power-down, the RESET outputs will be active when V_{CC} falls below V_{TH}. The $\overline{\text{RESET}}$ output will be valid so long as V_{CC} is >1.0 V (V_{RVALID}). The device is designed to ignore the fast negative going V_{CC} transient pulses (glitches).

Reset output timing is shown in Figure 1.

Manual Reset Operation

The $\overline{\text{RESET}}$ pin can operate as reset output and manual reset input. The input is edge triggered; that is, the $\overline{\text{RESET}}$ input will initiate a reset timeout after detecting a high to low transition.

When $\overline{\text{RESET}}$ I/O is driven to the active state, the 200 ms timer will begin to time the reset interval. If external reset is shorter than 200 ms, Reset outputs will remain active at least 200 ms.

The CAT1024/25 also have a separate manual reset input. Driving the $\overline{\text{MR}}$ input low by connecting a pushbutton (normally open) from $\overline{\text{MR}}$ pin to GND will generate a reset condition. The input has an internal pull up resistor.

Reset remains asserted while $\overline{\text{MR}}$ is low and for the Reset Timeout period after $\overline{\text{MR}}$ input has gone high.

Glitches shorter than 100 ns on $\overline{\text{MR}}$ input will not generate a reset pulse. No external debouncing circuits are required. Manual reset operation using $\overline{\text{MR}}$

EMBEDDED EEPROM OPERATION

The CAT1024 and CAT1025 feature a 2-kbit embedded serial EEPROM that supports the I^2C Bus data transmission protocol. This Inter-Integrated Circuit Bus protocol defines any device that sends data to the bus to be a transmitter and any device receiving data to be a receiver. The transfer is controlled by the Master device which generates the serial clock and all START and

ACKNOWLEDGE

After a successful data transfer, each receiving device is required to generate an acknowledge. The acknowledging device pulls down the SDA line during the ninth clock cycle, signaling that it received the 8 bits of data.

The CAT1024/25 responds with an acknowledge after receiving a START condition and its slave address. If the device has been selected along with a write operation, it responds with an acknowledge after receiving each 8-bit byte.

When the CAT1024/25 begins a READ mode it transmits 8 bits of data, releases the SDA line and monitors the line for an acknowledge. Once it receives this acknowledge, the CAT1024/25 will continue to transmit data. If no acknowledge is sent by the Master, the device terminates data transmis–sion and waits for a STOP condition.

WRITE OPERATIONS

Byte Write

In the Byte Write mode, the Master device sends the START condition and the slave address information (with the R/$\overline{W}$ bit set to zero) to the Slave device. After the Slave generates an acknowledge, the Master sends a 8-bit address that is to be written into the address pointers of the device. Afte

Acknowledge Polling

Disabling of the inputs can be used to take advantage of the typical write cycle time. Once the stop condition is issued to indicate the end of the host's write opration, the CAT1024/25 initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If the device is still busy with the write operation, no ACK will be returned. If a write operation has completed, an ACK will be returned and the host can then proceed with the next read or write operation.

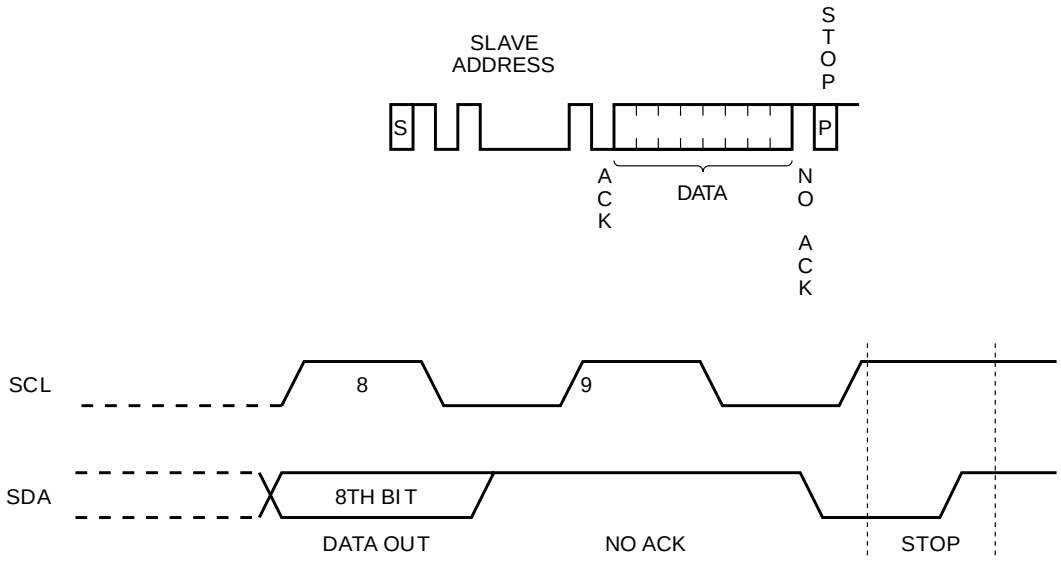
WRITE PROTECTION PIN (WP)

The Write Protection feature (CAT1025 only) allows the user to protect against inadvertent memory array programming. If the WP pin is tied to V_{CC}, the entire memory array is protected and becomes read only. The CAT1025 will accept both slave and byte addresses, but the memory location accessed is protected from programming by the device's failure to send an acknowledge after the first byte of data is received.

READ OPERATIONS

The READ operation for the CAT1024/25 is initiated in the same manner as the write operation with one exception, the R/$\overline{W}$ bit is set to one. Three different READ operations are possible: Immediate/Current Address READ, Selective/Random READ and Sequential READ.

Figure 10. Immediate Address Read Timing



Immediate/Current Address Read

The CAT1024 and CAT1025 address counter contains the address of the last byte accessed, incremented by one. In other words, if the last READ or WRITE access was to address N, the READ immediately following would access data from address N + 1. For N = E = 255, the counter will wrap around to zero and continue to clock out valid data. After the CAT1024/1025 receives its slave address information (with the R/$\overline{W}$ bit set to one), it issues an acknowledge, then transmits the 8-bit byte requested. The master device does not send an acknowledge, but will generate a STOP condition.

Selective/Random Read

Selective/Random READ operations allow the Master device to select at random any memory location for a READ operation. The Master device first performs a 'dummy' write operation by sending the START condition, slave address and byte addresses of the location it wishes to read. After the CAT1024 and CAT1025 acknowledges, the Master device sends the START condition and the slave address again, this time with the R/$\overline{W}$ bit set to one. The CAT1024 and CAT1025 then responds with its acknowledge and sends the 8-bit byte requested. The master device does not send an acknowledge but will generate a STOP condition.

Sequential Read

The Sequential READ operation can be initiated by either the Immediate Address READ or Selective READ operations. After the CAT1024 and CAT1025 sends the inital 8-bit byte requested, the Master will responds with an acknowledge which tells the device it requires more data. The CAT1024 and CAT1025 will continue to output an 8-bit byte for each acknowledge, thus sending the STOP condition.

The data being transmitted from the CAT1024 and CAT1025 is sent sequentially with the data from address N followed by data from address N + 1. The READ operation address counter increments all of the CAT1024 and CAT1025 address bits so that the entire memory array can be read during one operation.

Figure 11. Selective Read Timing

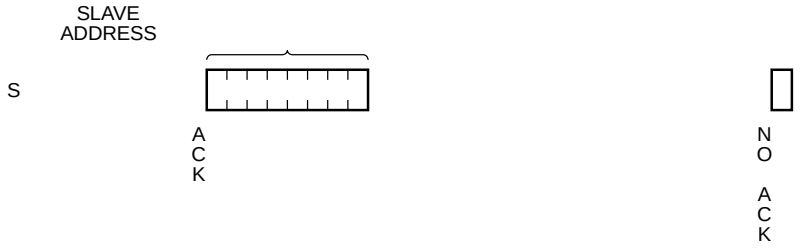
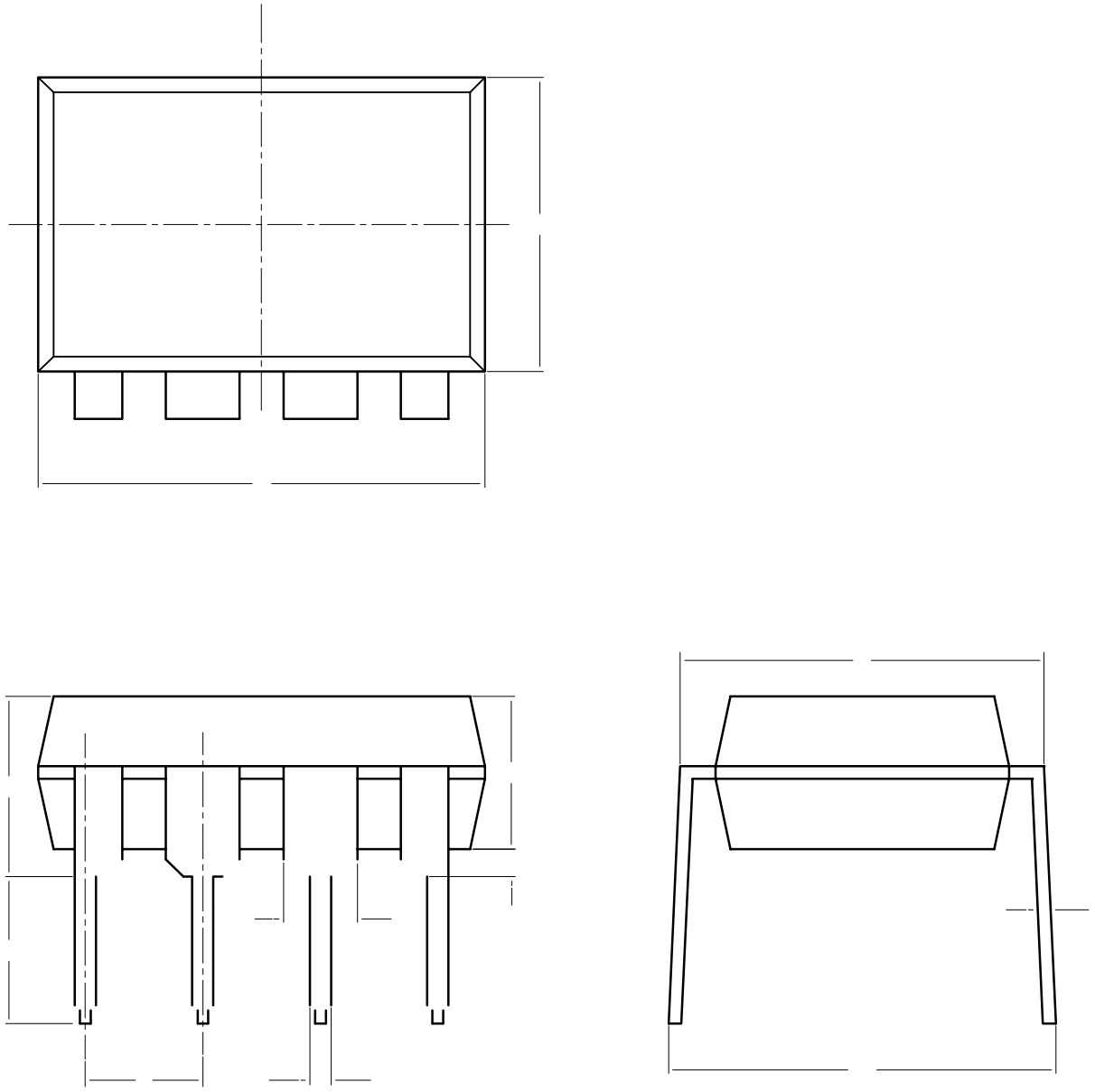


Figure 12. Sequential Read Timing

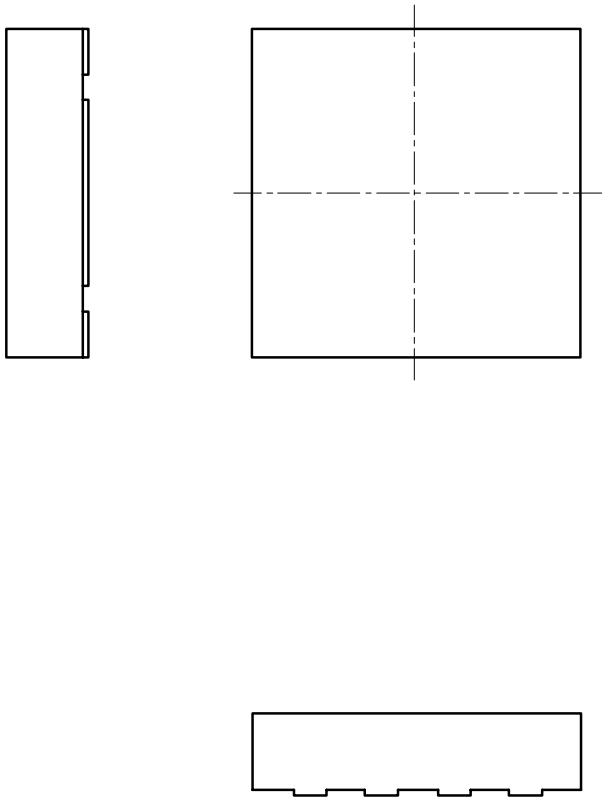
PACKAGE OUTLINE DRAWINGS

PDIP 8-Lead 300 mils (L)[(1)(2)]



Notes:
(1) All dimensions are in millimeters.
(2) Complies with JEDEC MS-001.

TDFN 8-Pad 3 x 3 mm (ZD4) [(1)(2)]



Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-229.

EXAMPLE OF ORDERING INFORMATION

ORDERING INFORMATION

Orderable Part Number – CAT1024xx	
CAT1024LI-45-G	CAT1024ZI-45-GT3
CAT1024LI-42-G	CAT1024ZI-42-GT3
CAT1024LI-30-G	CAT1024ZI-30-GT3

Orderable Part Number – CAT1025xx	
CAT1025LI-45-G	CAT1025ZI-45-GT3
CAT1025LI-42-G	CAT1025ZI-42-GT3
CAT1025LI-30-G	CAT1025ZI-30-GT3

REVISION HISTORY

Date	Rev.	Description
7-Nov-03	I	Eliminated Automotive temperature range
12-Apr-04	J	Eliminated data sheet designation Updated Reel Ordering Information
1-Nov-04	K	Changed SOIC package designators Eliminated 8-pad TDFN (3 x0.02 690 10.02 69.9A rec 9.317 1.15pf/CS0 cso9Fn 0.96 26.88 re5(rome

PUBLICATION ORDERING INFORMATION
LITERATURE FULFILLMENT:

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