Supervisory Circuits with EEPROM Serial 2k-bit I²C and Manual Reset

Description

The CAT1024 and CAT1025 are complete memory and supervisory solutions for microcontroller based systems. A 2k bit serial EEPROM memory and a system power supervisor with brown out protection are integrated together in low power CMOS technology. Memory interface is via a 400 kHz I²C bus.

The CAT1025 provides a precision Vcc sense circuit and two open drain outputs: one (RESET) drives high and the other (RESET) drives low whenever Vcc falls below the reset threshold voltage. The CAT1025 also has a Write Protect input (WP). Write operations are disabled if WP is connected to a logic high.

The CAT1024 also provides a precision V_{CC} sense circuit, but has only a RESET output and does not have a Write Protect input.

All supervisors have a 1.6 second watchdog timer circuit that resets a system to a known state if software or a hardware glitch halts or "hangs" the system. For the CAT1024 and CAT1022, the watchdog timer monitors the SDA signal. The CAT1023 has a separate watchdog timer interrupt input pin, WDI.

The power supply monitor and reset circuit protect memory and system controllers during power up/down and against brownout conditions. Five reset threshold voltages support 5 V, 3.3 V and 3 V systems. If power supply voltages are out of tolerance reset signals become active, preventing the system microcontroller, ASIC or peripherals from operating. Reset signals become inactive typically 200 ms after the supply voltage exceeds the reset threshold level. With both active high and low reset signals, interface to microcontrollers and other ICs is simple. In addition, the RESET pin or a separate input, MR, can be used as an input for push button manual reset capability.

The CAT1024/25 memory features a 16 byte page. In addition, hardware data protection is provided by a Vcc sense circuit that prevents writes to memory whenever Vcc falls below the reset threshold or until Vcc reaches the reset threshold during power up.

Available packages include a surface mount 8 pin SOIC, 8 pin TSSOP, 8 pin TDFN and 8 pin MSOP packages. The TDFN package thickness is 0.8 mm maximum. TDFN footprint is 3 x 3 mm.

Features

- Precision Power Supply Voltage Monitor
 - 5 V, 3.3 V and 3 V Systems
 - Five Threshold Voltage Options
- Active High or Low Reset
 - Valid Reset Guaranteed at Vcc = 1 V
- 400 kHz I²C Bus
- 2.7 V to 5.5 V Operation
- Low Power CMOS Technology
- 16 Byte Page Write Buffer

- Built in Inadvertent Write Protection
 - WP Pin (CAT1025)
- 1,000,000 Program/Erase Cycles
- Manual Reset Input
- 100 Year Data Retention
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PIN CONFIGURATION



(Bottom View) TDFN Package: 3 mm x 3 mm 0.8mm maximum height – (ZD4)



Table 4. CAT102X FAMILY OVERVIEW

Device	Manual Reset Input Pin	Watchdog	Watchdog Monitor Pin	Write Protection Pin	Independent Auxiliary Voltage Sense	RESET: Active High and LOW	EEPROM
CAT1021	~	\checkmark	SDA	~		1	2k
CAT1022	~	\checkmark	SDA				2k
CAT1023	1	\checkmark	WDI			1	2k
CAT1024	~						2k
CAT1025	~			~		1	2k
CAT1026					~	1	2k
CAT1027		\checkmark	WDI		~		2k

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

SPECIFICATIONS

Table 5. ABSOLUTE MAXIMUM RATINGS

Parameters	Ratings	Units
Temperature Under Bias	-55 to +125	°C
Storage Temperature	-65 to +150	°C
Voltage on any Pin with Respect to Ground (Note 1)	–2.0 to V _{CC} + 2.0	V
V _{CC} with Respect to Ground	-2.0 to 7.0	V
Package Power Dissipation Capability ($T_A = 25^{\circ}C$)	1.0	W
Lead Soldering Temperature (10 s)	300	°C

Table 6. D.C. OPERATING CHARACTERISTICS

V_{CC} = 2.7 V to 5.5 V and over the recommended temperature conditions unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
V _{TH}	Reset Threshold	CAT102x-45 (V _{CC} = 5.0 V)	4.50		4.75	V
		CAT102x-42 (V _{CC} = 5.0 V)	4.25		4.50	
		CAT102x-30 (V _{CC} = 3.3 V)	3.00		3.15	
		CAT102x-28 (V _{CC} = 3.3 V)	2.85		3.00	
		CAT102x-25 (V _{CC} = 3.0 V)	2.55		2.70	
V _{RVALID}	Reset Output Valid V _{CC} Voltage		1.00			V
V _{RT} (Note 4)	Reset Threshold Hysteresis		15			mV

V_{IL} min and V_{IH} max are reference values only and are not tested.
This parameter is tested initially and after a design or process change that affects the parameter. Not 100% tested.

Table 7. CAPACITANCE

 T_{A} = 25°C, f = 1.0 MHz, V_{CC} = 5 V

Symbol	Test	Test Conditions	Max	Units
C _{OUT} (Note 5)	Output Capacitance	V _{OUT} = 0 V	8	pF
C _{IN} (Note 5)	Input Capacitance	V _{IN} = 0 V	6	pF

Table 8. AC CHARACTERISTICS

V_{CC} = 2.7 V to 5.5 V and over the recommended temperature conditions, unless otherwise specified.

Memory Read & Write Cycle (Note 6)

Symbol	Parameter	Min	Max	Units
f _{SCL}	Clock Frequency		400	kHz
t _{SP}	Input Filter Spike Suppression (SDA, SCL)		100	ns
t _{LOW}	Clock Low Period	1.3		μs
tнідн	Clock High Period	0.6		μs
t _R (Note 5)	SDA and SCL Rise Time		300	ns
t _F (Note 5)	SDA and SCL Fall Time		300	ns
t _{HD;} STA	Start Condition Hold Time	0.6		μs
t _{SU;} STA	Start Condition Setup Time (for a Repeated Start)	0.6		μs
t _{HD;} DAT	Data Input Hold Time	0		ns
t _{SU; DAT}	Data Input Setup Time	100		ns
t _{SU;} sto	Stop Condition Setup Time	0.6		μs
t _{AA}	SCL Low to Data Out Valid		900	ns
t _{DH}	Data Out Hold Time	50		ns
t _{BUF} (Note 5)	Time the Bus must be Free Before a New Transmission Can Start	1.3		μs
t _{WC} (Note 7)	Write Cycle Time (Byte or Page)		5	ms

5. This parameter is characterized initially and after a design or process change that affects the parameter. Not 100% tested.

6. Test Conditions according to "AC Test Conditions" table.

7. The write cycle time is the time from a valid stop condition of a write sequence to the end of the internal program/erase cycle. During the write cycle, the bus interface circuits are disabled, SDA is allowed to remain high and the device does not respond to its slave address.

Table 9. RESET CIRCUIT AC CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
t _{PURST}	Power–Up Reset Timeout	Note 2	130	200	270	ms
t _{RDP}	V _{TH} to RESET output Delay	Note 3			5	μs
t _{GLITCH}	V _{CC} Glitch Reject Pulse Width	Notes 4 and 5			30	ns
MR Glitch	Manual8.40659.8 137.h7munity	Note 1			100	ns
t _{MRW}	MR Pulse Width	Note 1	5			μs
t _{MRD}	MR Input to RESET Output Delay	Note 1			1	μs

Table 10. POWER-UP TIMING (Notes 5 and 6)

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
t _{PUR}	Power–Up to Read Operation				270	ms
t _{PUW}	Power–Up to Write Operation				270	ms

Table 11. AC TEST CONDITIONS

Parameter	Test Conditions
Input Pulse Voltages	0.2 x V _{CC} to 0.8 x V _{CC}
Input Rise and Fall Times	10 ns
Input Reference Voltages	0.3 x V _{CC} , 0.7 x V _{CC}
Output Reference Voltages	0.5 x V _{CC}
Output Load	Current Source: I_{OL} = 3 mA; C_L = 100 pF

Table 12. RELIABILITY CHARACTERISTICS

Symbol	Parameter	Reference Test Method	Min	Max	Units
N _{END} (Note 5)	Endurance	MIL-STD-883, Test Method 1033	1,000,000		Cycles/Byte
T _{DR} (Note 5)	Data Retention	MIL-STD-883, Test Method 1008	100		Years
V _{ZAP} (Note 5)	ESD Susceptibility	MIL-STD-883, Test Method 3015	2000		Volts
I _{LTH} (Notes 5 & 7)	Latch–Up	JEDEC Standard 17	100		mA

1. Test Conditions according to "AC Test Conditions" table.

DEVICE OPERATON

Reset Controller Description

The CAT1024/25 precision RESET controllers ensure correct system operation during brownout and power up/down conditions. They are configured with open drain RESET outputs.

During power up, the RESET outputs remain active until Vcc reaches the VTH threshold and will continue driving the outputs for approximately 200 ms (tPURST) after reaching VTH. After the tPURST timeout interval, the device will cease to drive the reset outputs. At this point the reset outputs will be pulled up or down by their respective pull up/down resistors.

During power down, the RESET outputs will be active when Vccfalls below VTH. The RESET output will be valid so long as Vcc is > 1.0 V (VRVALID). The device is designed to ignore the fast negative going Vcc transient pulses (glitches).

Reset output timing is shown in Figure 1.

Manual Reset Operation

The RESET pin can operate as reset output and manual reset input. The input is edge triggered; that is, the RESET input will initiate a reset timeout after detecting a high to low transition.

When RESET I/O is driven to the active state, the 200 ms timer will begin to time the reset interval. If external reset is shorter than 200 ms, Reset outputs will remain active at least 200 ms.

The CAT1024/25 also have a separate manual reset input. Driving the \overline{MR} input low by connecting a pushbutton (normally open) from \overline{MR} pin to GND will generate a reset condition. The input has an internal pull up resistor.

Reset remains asserted while \overline{MR} is low and for the Reset Timeout period after \overline{MR} input has gone high.

Glitches shorter than 100 ns on $\overline{\text{MR}}$ input will not generate a reset pulse. No external debouncing circuits are required. Manual reset operation using $\overline{\text{MR}}$ input is shown in Figure 2.

Hardware Data Protection

The CAT1024/25 supervisors have been designed to solve many of the data corruption issues that have long been associated with serial EEPROMs. Data corruption occurs when

EMBEDDED EEPROM OPERATON

The CAT1024 and CAT1025 feature a 2 kbit embedded serial EEPROM that supports the I²C Bus data transmission protocol. This Inter Integrated Circuit Bus protocol defines any device that sends data to the bus to be a transmitter and any device receiving data to be a receiver. The transfer is controlled by the Master device which generates the serial clock and all START and STOP conditions for bus access. Both the Master device and Slave device can operate as either transmitter or receiver, but the Master device controls which mode is activated.

I²C Bus Protocol

The features of the I^2C bus protocol are defined as follows:

1. Data transfer may be initiated only when the bus is not busy.

2. During a data transfer, the data line must remain stable whenever the clock line is high. Any changes in the data line while the clock line is high will be interpreted as a START or STOP condition.

Start Condition

The START Condition precedes all commands to the device, and is defined as a HIGH to LOW transition of SDA when SCL is HIGH. The CAT1024/25 monitors the SDA and SCL lines and will not respond until this condition is met.

Stop Condition

A LOW to HIGH transition of SDA when SCL is HIGH determines the STOP condition. All operations must end with a STOP condition.

DEVICE ADDRESSING

The Master begins a transmission by sending a START condition. The Master sends the address of the particular slave device it is requesting. The four most significant bits of the 8 bit slave address are programmable in metal and the default is 1010.

The last bit of the slave address specifies whether a Read or Write operation is to be performed. When this bit is set to 1, a Read operation is selected, and when set to 0, a Write operation is selected. After the Master sends a START condition and the slave address byte, the CAT1024/25 monitors the bus and responds with an acknowledge (on the SDA line) when its address matches the transmitted slave address. The CAT1024/25 then perform a Read or Write operation depending on the R/W bit.



Figure 3. Bus Timing

ACKNOWLEDGE

After a successful data transfer, each receiving device is required to generate an acknowledge. The acknowledging device pulls down the SDA line during the ninth clock cycle, signaling that it received the 8 bits of data.

The CAT1024/25 responds with an acknowledge after

Page Write



Figure 10. Immediate Address Read Timing

Immediate/Current Address Read

The CAT1024 and CAT1025 address counter contains the address of the last byte accessed, incremented by one. In other words, if the last READ or WRITE access was to address N, the READ immediately following would access data from address N + 1. For N = E = 255, the counter will wrap around to zero and continue to clock out valid data. After the CAT1024/1025 receives its slave address information (with the R/W bit set to one), it issues an acknowledge, then transmits the 8 bit byte requested. The master device does not send an acknowledge, but will generate a STOP condition.

Selective/Random Read

Selective/Random READ operations allow the Master device to select at random any memory location for a READ operation. The Master device first performs a 'dummy' write operation by sending the START condition, slave address and byte addresses of the location it wishes to read. After the CAT1024 and CAT1025 acknowledges, the Master device sends the START condition and the slave address again, this time with the R/W bit set to one. The CAT1024 and CAT1025 then responds with its acknowledge and sends the 8 bit byte requested. The master device does not send an acknowledge but will generate a STOP condition.

Sequential Read

The Sequential READ operation can be initiated by either the Immediate Address READ or Selective READ operations. After the CAT1024 and CAT1025 sends the initial 8 bit byte requested, the Master will responds with an acknowledge which tells the device it requires more data. The CAT1024 and CAT1025 will continue to output an 8 bit byte for each acknowledge, thus sending the STOP condition.

The data being transmitted from the CAT1024 and CAT1025 is sent sequentially with the data from address N followed by data from address N + 1. The READ operation address counter increments all of the CAT1024 and CAT1025 address bits so that the entire memory array can be read during one operation.



Figure 11. Selective Read Timing



Figure 12. Sequential Read Timing

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ORDERING INFORMATION

Orderable Part Numbers

SOIC-8, 150 mils CASE 751BD ISSUE O

DATE 19 DEC 2008





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