miconductor®

Supervisory Circuits with I²C Serial 2k-bit CMOS EEPROM, Manual Reset and Watchdog Timer

FEATURES

- Â **Precision Power Supply Voltage Monitor**
  - **— 5 V, 3.3 V and 3 V systems**
  - **— Five threshold voltage options**
- Â **Watchdog Timer**
- Â **Active High or Low Reset**
  - **— Valid reset guaranteed at V_{CC} = 1 V**
- Â **400 kHz I²C Bus**
- Â **2.7 V to 5.5 V Operation**
- Â **Low power CMOS technology**
- Â **16-Byte Page Write Buffer**
- Â **Built-in inadvertent write protection**
  - **— WP pin (CAT1021)**
- Â **1,000,000 Program/Erase cycles**
- Â **Manual Reset Input**
- Â **100 year data retention**
- Â **Industrial and extended temperature ranges**
- Â **8-pin DIP, SOIC, TSSOP, MSOP or TDFN (3 x 3 mm foot-print) packages — WP Twrm81 Tf004 a 3 a 3 e**

BLOCK DIAGRAM

THRESHOLD VOLTAGE OPTION

Part Dash Number	Minimum Threshold	Maximum Threshold

PIN DESCRIPTION

RESET/$\overline{\text{RESET}}$:

CAPACITANCE

T_A = 25ºC, f = 1.0 MHz, V_{CC} = 5 V

Symbol	Test	Test Conditions	Max	Units
C_{OUT} (1)	Output Capacitance	V_{OUT} = 0 V	8	pF
C_{IN} (1)	Input Capacitance	V_{IN} = 0 V	6	pF

AC CHARACTERISTICS

V_{CC} = 2.7 V to 5.5 V and over the recommended temperature conditions, unless otherwise specified.

Memory Read & Write Cycle(2)

Symbol	Parameter	Min	Max	Units
f_{SCL}	Clock Frequency		400	kHz
t_{SP}	Input Filter Spike Suppression (SDA, SCL)		100	ns
t_{LOW}	Clock Low Period	1.3		µs
t_{HIGH}	Clock High Period	0.6		µs
t_R (1)	SDA and SCL Rise Time		300	ns
t_F (1)	SDA and SCL Fall Time		300	ns
$t_{HD; STA}$	Start Condition Hold Time	0.6		µs
$t_{SU; STA}$	Start Condition Setup Time (for a Repeated Start)	0.6		µs
$t_{HD; DAT}$	Data Input Hold Time	0		ns
$t_{SU; DAT}$	Data Input Setup Time	100		ns
$t_{SU; STO}$	Stop Condition Setup Time	0.6		µs
t_{AA}	SCL Low to Data Out Valid		900	ns
t_{DH}	Data Out Hold Time	50		ns
t_{BUF} (1)	Time the Bus must be Free Before a New Transmission Can Start	1.3		µs
t_{WC} (3)	Write Cycle Time (Byte or Page)		5	ms

Notes:

(1) This parameter is characterized initially and after a design or process change that affects the parameter. Not 100% tested.

(2) Test Conditions according to “AC Test Conditions” table.

(3) The write cycle time is the time from a valid stop condition of a write sequence to the end of the internal program/erase cycle. During the write cycle, the bus interface circuits are disabled, SDA is allowed to remain high and the device does not respond to its slave address.

RESET CIRCUIT AC CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
t_{PURST}	Power-Up Reset Timeout	Note 2	130	200	270	ms
t_{RDP}	V_{TH} to RESET output Delay	Note 3			5	µs
t_{GLITCH}	V_{CC} Glitch Reject Pulse Width	Note 4, 5			30	ns
MR Glitch	Manual Reset Glitch Immunity	Note 1			100	ns
t_{MRW}	MR Pulse Width	Note 1	5			µs
t_{MRD}	MR Input to RESET Output Delay	Note 1			1	µs
t_{WD}	Watchdog Timeout	Note 1	1.0	1.6	2.1	sec

POWER-UP TIMING [5], [6]

DEVICE OPERATION

Reset Controller Description

The CAT1021/22/23 precision RESET controllers ensure correct system operation during brownout and power up/down conditions. They are configured with open drain RESET outputs.

During power-um5ut notice

EMBEDDED EEPROM OPERATION

The CAT1021/22/23 feature a 2-kbit embedded serial EEPROM that supports the I^2C Bus data transmission protocol. This Inter-Integrated Circuit Bus protocol defines any device that sends data to the bus to be a transmitter and any device receiving data to be a receiver. The transfer is controlled by the Master device which generates the serial clock and all START and STOP conditions for bus access. Both the Master device and Slave device can operate as either transmitter or receiver, but the Master device controls which mode is activated.

I^2C BUS PROTOCOL

The features of the I^2C bus protocol are defined as follows:

(1) Data transfer may be initiated only when the bus is not busy.
(2) During a data transfer, the data line must remain stable whenever the clock line is high. Any changes in the data line while the clock line is high will be interpreted as a START or STOP condition.

START CONDITION

The START Condition precedes all commands to the device, and is defined as a HIGH to LOW transition of SDA when SCL is HIGH. The CAT1021/22/23 monitor the SDA and SCL lines and will not respond until this condition is met.

STOP CONDITION

A LOW to HIGH transition of SDA when SCL is HIGH determines the STOP condition. All operations must end with a STOP condition.

DEVICE ADDRESSING

The Master begins a transmission by sending a START condition. The Master sends the address of the particular slave device it is requesting. The four most significant bits of the 8-bit slave address are programmable in metal and the default is 1010.

The last bit of the slave address specifies whether a Read or Write operation is to be performed. When this bit is set to 1, a Read operation is selected, and when set to 0, a Write operation is selected.

After the Master sends a START condition and the slave address byte, the CAT1021/22/23 monitors the bus and responds with an acknowledge (on the SDA line) when its address matches the transmitted slave address. The CAT1021/22/23 then perform a Read or Write operation depending on the R/$\overline{W}$ bit.

Figure 3. Bus Timing

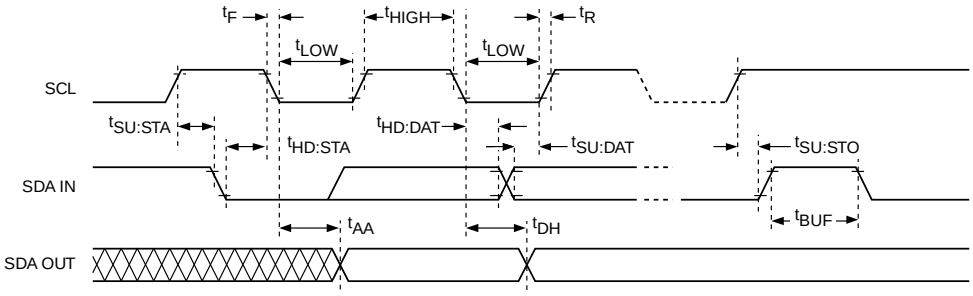
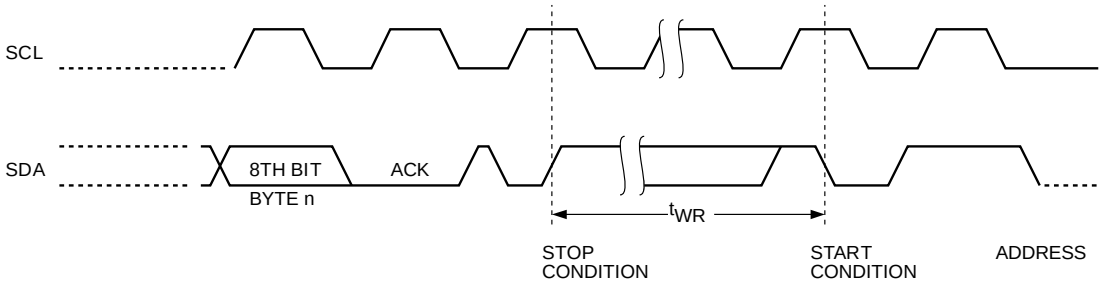


Figure 4. Write Cycle Timing



ACKNOWLEDGE

After a successful data transfer, each receiving device is required to generate an acknowledge. The acknowledging device pulls down the SDA line during the ninth clock cycle, signaling that it received the 8 bits of data.

All devices respond with an acknowledge after receiving a START condition and its slave address. If the device has been selected along with a write operation, it responds with an acknowledge after receiving each 8-bit byte.

When a device begins a READ mode it transmits 8 bits of data, releases the SDA line and monitors the line for an acknowledge. Once it receives this acknowledge, the device will continue to transmit data. If no acknowledge is sent by the Master, the device terminates data transmission and waits for a STOP condition.

WRITE OPERATIONS

Byte Write

In the Byte Write mode, the Master device sends the START condition and the slave address information (with the R/$\overline{W}$ bit set to zero) to the Slave device. After the Slave generates an acknowledge, the Master sends a 8-bit address that is to be written into the address pointers of the device. After receiving another acknowledge from the Slave, the Master device transmits the data to be written into the addressed memory location. The device acknowledges once more and the Master generates the STOP condition. At this time, the device begins an internal programming cycle to non-volatile memory. While the cycle is in progress, the device will not respond to any request from the Master device.

Figure 5. Start/Stop Timing

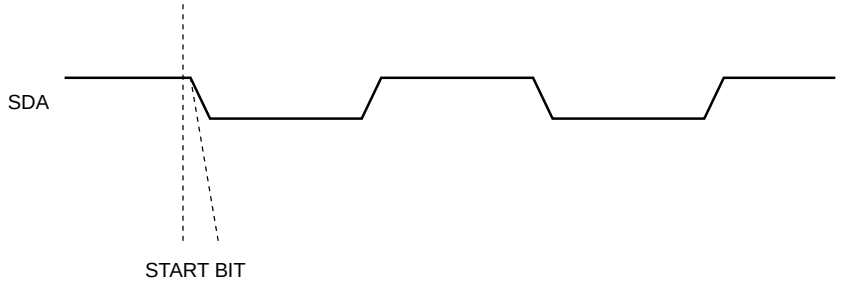


Figure 6. Acknowledge Timing

Figure 7: Slave Address Bits

Page Write

The CAT1021/22/23 writes up to 16 bytes of data in a single write cycle, using the Page Write operation. The page write operation is initiated in the same manner as the byte write operation, however instead of terminating after the init

Acknowledge Polling

Disabling of the inputs can be used to take advantage of the typical write cycle time. Once the stop condition is issued to indicate the end of the host's write opration, the CAT1021/22/23 initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If the device is still busy with the write operation, no ACK will be returned. If a write operation has completed, an ACK will be returned and the host can then proceed with the next read or write operation.

Immediate/Current Address Read

The CAT1021/22/23 address counter contains the address of the last byte accessed, incremented by one. In other words, if the last READ or WRITE access was to address N, the READ immediately following would access data from address N + 1. For N = E = 255, the counter will wrap around to zero and continue to clock out valid data. After the CAT1021/22/23 receives its slave address information (with the R/$\overline{W}$ bit set to one), it issues an acknowledge, then transmits the 8-bit byte requested. The master device does not send an acknowledge, but will generate a STOP condition.

Selective/Random Read

Selective/Random READ operations allow the Master device to select at random any memory location for a READ operation. The Master device first performs a 'dummy' write operation by sending the START condition, slave address and byte addresses of the location it wishes to read. After the CAT1021/22/23 acknowledges, the Master device sends the START condition and the slave address again, this time with the R/$\overline{W}$ bit set to one. The CAT1021/22/23 then responds with its acknowledge and sends the 8-bit byte requested. The master device does not send an acknowledge but will generate a STOP condition.

Sequential Read

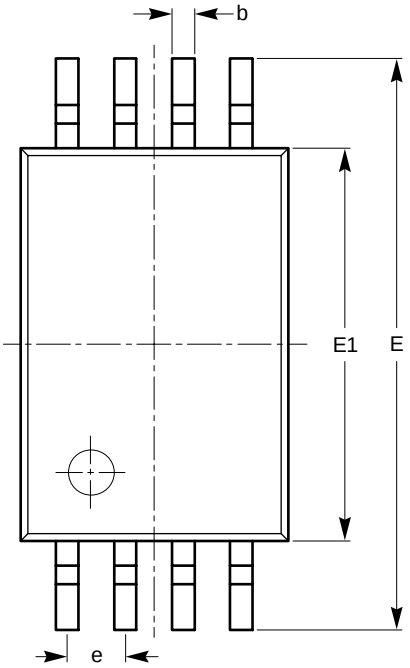
The Sequential READ operation can be initiated by either the Immediate Address READ or Selective READ operations. After the CAT1021/22/23 sends the inital 8-bit byte requested, the Master will responds with an acknowledge which tells the device it requires more data. The CAT1021/22/23 will continue to output an 8-

PACKAGE OUTLINE DRAWINGS

PDIP 8-Lead 300 mils (L)[(1)(2)]

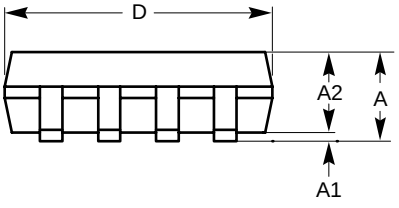
Notes:
(1) All dimensions are in millimeters.
(2) Complies with JEDEC MS-001.

TSSOP 8-Lead (V) (1)(2)

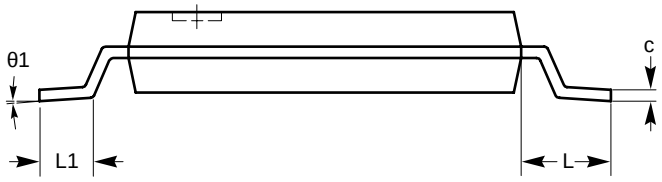


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			1.20
A1	0.05		0.15
A2	0.80	0.90	1.05
b	0.19		0.30
c	0.09		0.20
D	2.90	3.00	3.10
E	6.30	6.40	6.50
E1	4.30	4.40	4.50
e	0.65 BSC		
L	1.00 REF		
L1	0.50	0.60	0.75
θ1	0°		8°



SIDE VIEW



END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-153

Orderable Part Number – CAT1022xx	
CAT1022LI-45-G	CAT1022ZI-45-GT3
CAT1022LI-42-G	CAT1022ZI-42-GT3
CAT1022LI-30-G	CAT1022ZI-30-GT3
CAT1022LI-28-G	CAT1022ZI-28-GT3
CAT1022LI-25-G	CAT1022ZI-25-GT3
CAT1022WI-45-GT3	CAT1022ZD4I-45T3*
CAT1022WI-42-GT3	CAT1022ZD4I-42T3*
CAT1022WI-30-GT3	CAT1022ZD4I-30T3*
CAT1022WI-28-GT3	CAT1022ZD4I-28T3*
CAT1022WI-25-GT3	CAT1022ZD4I-25T3*
CAT1022YI-45-GT3	
CAT1022YI-42-GT3	
CAT1022YI-30-GT3	
CAT1022YI-28-GT3	
CAT1022YI-25-GT3	

* Part number is not exactly the same as the “Example of Ordering Information” shown on page 19. For part numbers marked with ***** there is only one hyphen in the orderable part number, which is placed before the “Reset Threshold Voltage”.

Orderable Part Number – CAT1023xx	
CAT1023LI-45-G	CAT1023ZI-45-GT3
CAT1023LI-42-G	CAT1023ZI-42-GT3
CAT1023LI-30-G	CAT1023ZI-30-GT3
CAT1023LI-28-G	CAT1023ZI-28-GT3
CAT1023LI-25-G	CAT1023ZI-25-GT3
CAT1023WI-45-GT3	CAT1023ZD4I-45T3*
CAT1023WI-42-GT3	CAT1023ZD4I-42T3*
CAT1023WI-30-GT3	CAT1023ZD4I-30T3*
CAT1023WI-28-GT3	CAT1023ZD4I-28T3*
CAT1023WI-25-GT3	CAT1023ZD4I-25T3*
CAT1023YI-45-GT3	
CAT1023YI-42-GT3	
CAT1023YI-30-GT3	
CAT1023YI-28-GT3	
CAT1023YI-25-GT3	

* Part number is not exactly the same as the “Example of Or

REVISION HISTORY

Date	Rev.	Reason
25-Sep-03	F	Added Green Package logo Updated DC Operating Characteristic notes Updated Reliability Characteristics notes
7-Nov-03	G	Eliminated Automotive temperature range Updated Ordering Information with “Green” package codes Updated Reset Circuit AC Characteristics
4-Dec-04	H	Eliminated data sheet designation Updated Reel Ordering Information
11-Jan-04	I	Eliminated 8-pad TDFN package (3 x 4.9 mm) Changed SOIC package designators Added package outlines
11-Apr-04	J	Update Pin Configuration
11-Nov-04	K	Update Feature Update Description Update DC Operating Characteristic Update AC Characteristics
3-Feb-07	L	Update Example of Ordering Information
28-Nov/07	M	Update Package Outline Drawings Update Example of Ordering Information Add “MD-“ to document number
3-Nov-08	N	Change logo and fine print to ON Semiconductor
5-Mar-09	O	Update Ordering Information (Remove 2,000/Reel)
14-Jul-09	P	Update Ordering Information table

PUBLICATION ORDERING INFORMATION
LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
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