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Integrated A/D Converters and Powered Output: minimize need for external components Flexible Clocking Architecture: supports speeds up to 40 MHz	Data Security: sensitive program data can be encrypted for storage in external NVRAM to prevent unauthorized parties from gaining access to proprietary software intellectual property, 128 bit AES encryption
<ul> <li>"Smart" Power Management: including low current standby mode requiring only 0.06 mA</li> <li>Diverse Memory Architecture: 4864x48 bit words of shared memory between the CFX core and the HEAR accelerator plus 8 Kword DSP core data memory, 12 Kwords of 32 bit DSP core program memory as well as other memory banks</li> </ul>	<b>Development Tools:</b> interface hardware with USB support as well as a full IDE that can be used for every step of program development including testing and debugging These Devices are Pb Free, Halogen Free/BFR Free and are RoHS Compliant
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## FIGURES AND DATA

### Table 1. ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Max	Unit
Voltage at any input pin	-0.3	2.0	V
Operating supply voltage (Note 1)	0.9	2.0	V
Operating temperature range (Note 2)	-40	8540	

## Table 2. ELECTRICAL SPECIFICATIONS (continued)

Description	Symbol	Conditions	Min	Тур	Max	Units	Screened
VDBL (1 µF External Cap	acitor)	•	•		•		
Regulator PSRR	VDBL <sub>PSRR</sub>	1 kHz	35	41	_	dB	
Load current	I <sub>LOAD</sub>		-	-	2.5	mA	
Load regulation	LOAD <sub>REG</sub>		-	7	10	mV/mA	
Line regulation	LINE <sub>REG</sub>		-	10	20	mV/V	
VDDC (1 µF External Cap	acitor)						
Digital supply voltage output	VDDC	Configured by a control register	0.79	0.95	1.25	V	
VDDC output level adjustment	VDDC <sub>STEP</sub>		27	29	31	mV	
Regulator PSRR	VDDC <sub>PSRR</sub>	1 kHz	25	25.5	26	dB	
Load current	I <sub>LOAD</sub>		-	-	3.5	mA	
Load regulation	LOAD <sub>REG</sub>		-	3	12	mV/mA	
Line regulation	LINE <sub>REG</sub>		-	3	8	mV/V	

POWER-

WLCSP Pin Out

## Assembly / Design Notes

For PCB manufacture with BelaSigna 300, onsemi recommends solder on pad (SoP) surface finish. With SoP, the solder mask opening should be non solder mask defined (NSMD) and copper pad geometry will be dictated by the PCB vendor's design requirements.

Alternative surface finishes are ENiG and OSP; volume of screened solder paste (#5) should be less than 0.0008 mm<sup>3</sup>. If no pre screening of solder paste is used, then following conditions must be met:

## WLCSP Weight

BelaSigna 300 has an average weight of 0.095 grams.

#### **Recommended Circuit Design Guidelines**

BelaSigna 300 is designed to allow both digital and analog processing in a single system. Due to the mixed signal nature of this system, the careful design of the printed circuit board (PCB) layout is critical to maintain the high audio fidelity of BelaSigna 300. To avoid coupling noise into the audio signal path, keep the digital traces away from the analog traces. To avoid electrical feedback coupling, isolate the input traces from the output traces.

- 1. the solder mask opening should be >0.3 mm in diameter,
- 2. the copper pad will have 0.25 mm diameter, and
- 3. soldermask thickness should be less than 1 mil thick above the copper surface.

onsemi can provide BelaSigna 300 WLCSP land pattern CAD files to assist your PCB design upon request.

#### Recommended Ground Design Strategy

The ground plane should be partitioned into two: the analog ground plane (AGND) and the digital ground plane (DGND). These two planes should be connected together at a single point, known as the star point. The star point should be located at the ground terminal of a capacitor on the output of the power regulator as illustrated in Figure 1.

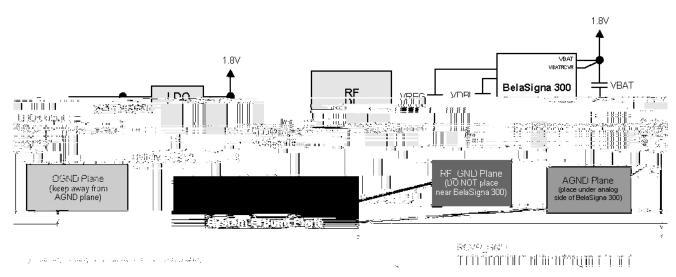


Figure 1. Schematic of Ground Scheme

#### Table 7. NON–CRITICAL SIGNALS

Pin Name	Description	Routing Guideline
CAP0, CAP1	Internal charge pump – capacitor connection	Place 100 nF capacitor close to pins
SDA, SCL	I2C port	Keep as short as possible
GPIO[30]	General-purpose I/O	Not critical
UART_RX, UART_TX	General-purpose UART	Not critical
PCM_FRAME, PCM_CLK, PCM_OUT, PCM_IN	PCM port	Keep away from analog input lines
LSAD[41]	Low-speed A/D converters	Not critical
SPI_CLK, SPI_CS, SPI_SERI, SPI_SERO	Serial peripheral interface port Connect to EEPROM	Keep away from analog input lines

#### **Audio Inputs**

The audio input traces should be as short as possible. The input impedance of each audio input pad (e.g., AI0, AI1, AI2, AI3, AI4) is high (approximately 500 k $\Omega$ ); therefore a 10 nF capacitor is sufficient to decouple the DC bias. This capacitor and the internal resistance form a first order analog high pass filter whose cutoff frequency can be calculated by  $f_{3dB}(Hz) = 1/(R \times C \times 2)$ , which results in ~30 Hz for a 10 nF capacitor. This 10 nF capacitor value applies when the preamplifier is being used, in other words, when a non unity gain is applied to the signals. When the preamplifier is by passed, the impedance is reduced; hence, the cut off frequency of the resulting high pass filter could be too high. In such a case, the use of a 30 40 nF serial capacitor is recommended. In cases where line level analog inputs without DC bias are used, the capacitor may be omitted for transparent bass response.

BelaSigna 300 provides microphone power supply (VREG) and ground (AGND). Keep audio input traces strictly away from output traces. A 2.0 V microphone bias might also be provided by the VDBL power supply.

Digital outputs (RCVR) MUST be kept away from microphone inputs to avoid cross coupling.

#### **Audio Outputs**

The audio output traces should be as short as possible. The trace length of RCVR+ and RCVR should be approximately the same to provide matched impedances.

### **Recommendation for Unused Pins**

The table below shows the recommendation for each pin when they are not used.

WLCSP Ball Index	BelaSigna 300 Signal Name	Recommended Connection when Not Used
B2	RCVR_HP+	Do not connect
C3	RCVR+	Do not connect
A3	RCVR-	Do not connect
B4	RCVR_HP-	Do not connect
A11	AI4	Connect to AGND
N/A	AI3/LOUT3	Connect to AGND
B12	AI2/LOUT2	Connect to AGND
A13	AI1/LOUT1	Connect to AGND
B14	AI0/LOUT0	Connect to AGND
D14	GPIO[4]/LSAD[4]	

#### Table 8. RECOMMENDATIONS FOR UNUSED PADS

## Table 8. RECOMMENDATIONS FOR UNUSED PADS (continued)

	WLCSP Ball Index	BelaSigna 300 Signal Name	Recommended Connection when Not Used
Γ	D6	SPI_CS	

## CFX DSP Core

The CFX DSP is a user programmable general purpose DSP core that uses a 24 bit fixed point, dual MAC, dual Harvard architecture. It is able to perform two MACs, two memory operations and two pointer updates per cycle, making it well suited to computationally intensive algorithms.

## The CFX features:

Dual MAC 24 bit load store DSP core

Four 56 bit accumulators

Four 24 bit input registers

Support for hardware loops nested up to 4 deep

Combined XY memory space (48 bits wide)

### Dual address generator units

Wide range of addressing modes:

Direct

Indirect with post modification Modulo addressing Bit reverse

## **CFX DSP Architecture**

The CFX architecture encompasses various memory types and sizes, peripherals, interrupt controllers, and interfaces. Figure 3 illustrates the basic architecture of the CFX. The control lines shown exiting the PCU indicate that control signals go from the PCU to essentially all other parts of the CFX.

The CFX employs a parallel instruction set for simultaneous control of multiple computation units. The DSP can execute up to four computation operations in parallel with two data transfers (including rounding and/or saturation as well as complex address updates), while simultaneously changing control flow.

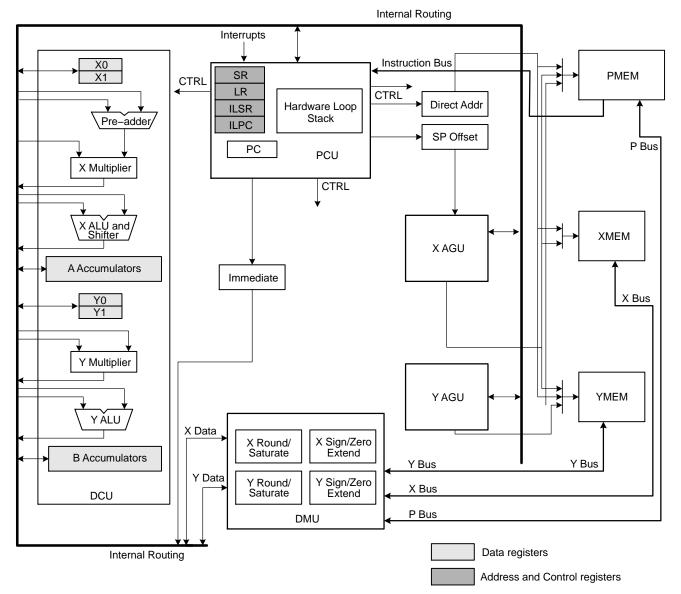


Figure 3. CFX DSP Core Architecture

## **CFX DSP Instruction Set**

Table 9 shows the list of all general CFX instructions and their description. Many instructions have multiple variations not shown in the table. Please refer to the CFX DSP Architecture Manual for more details.

## Table 9. CFX SUMMARY INSTRUCTION SET

Instruction	Description
ABS	Calculate the absolute value of a data register or accumulator
ADD	

Instruction	Description
RETURN	Return from a subroutine
RETURNI	Return from an interrupt
SHLL	Shift a data register left logically
SHRA	Shift a data register right arithmetically
SHRL	Shift a data register right logically
SLEEP	Enter sleep mode and wait for an interrupt and then wake up from sleep mode
STORE	Store data, a register or accumulator in a register, accumulator or memory location
SUB	Subtract two data registers or accumulators, storing the result in a data register or accumulator
SUBMUL	Subtract two XY data registers, multiply the result by a third XY data register, and store the result in an accumulator
SUBMULADD	Subtract two XY data registers, multiply the result by a third XY data register, and add the result to an accumulator
SUBMULNEG	Subtract two XY data registers, multiply the result by a third XY data register, negate the result and store it in an accumulator
SUBMULSUB	Subtract two XY data registers, multiply the result by a third XY data register, and subtract the result from an accumulator
SUBSH	Subtract two data registers or two accumulators and shift right one bit, storing the result in a data register or accumulator
SUBSTEP	Subtract a step register from the corresponding pointer
SWAP	Swap the contents of two data registers, conditionally
XOR	Perform a bitwise XOR operation on two data registers or a data register and a value, storing the result in a data register

#### HEAR Configurable Accelerator

The HEAR Configurable Accelerator is a highly optimized signal processing engine that is configured through the CFX. It offers high speed, high flexibility and high performance, while maintaining low power consumption. For added computing precision, the HEAR supports block floating point processing. Configuration of the HEAR is performed using the HEAR configuration tool (HCT). For further information on the usage of the HEAR and the HCT, please refer to the HEAR Configurable Accelerator Reference Manual.

R

## **Shared Memories**

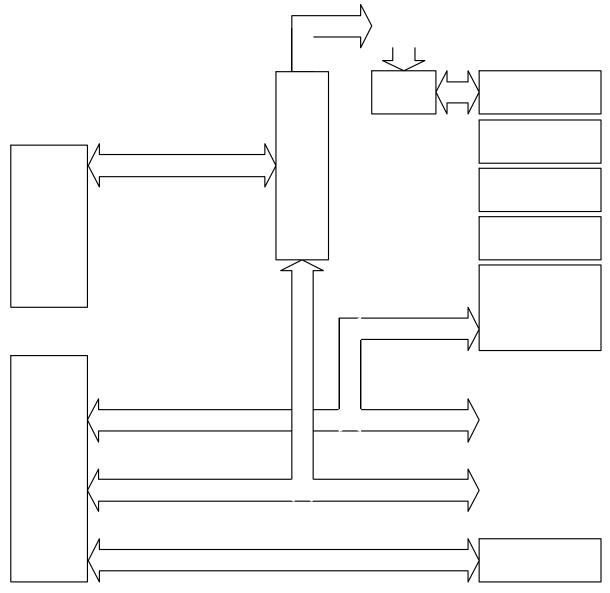
The shared CFX/HEAR memories include the following:

### Table 11. SHARED MEMORIES

Туре	Name	Size
Data memory (RAM)	H0MEM, H1MEM, H2MEM, H3MEM, H4MEM, H5MEM	Each 128x48-bit words
FIFO memory (RAM)	AMEM, BMEM	Each 1024x48-bit words
Coefficient memory (RAM)	CMEM, DMEM	Each 1024x48-bit words
Data ROM	SIN/COS LUT	512x48-bit words containing the 512 point sin/cos look up table
Microcode memory (RAM)	MICROCODE_MEM	2048x32-bit words

### **Memories Structure**

Figure 4 shows the system memory structure. The individual blocks are described in the sections that follow.



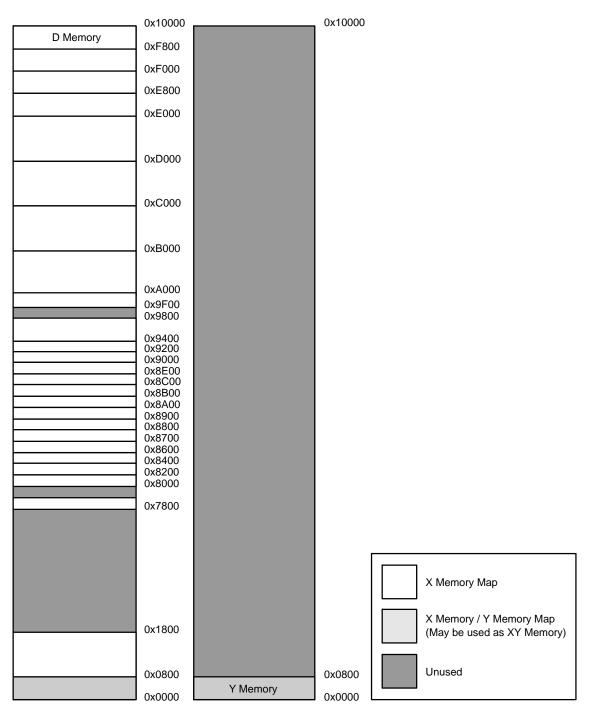


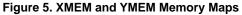
## **FIFO Controller**

The FIFO controller handles the moving of data to and from the FIFOs, after being initially configured. Up to eight FIFOs can be created by the FIFO controller, four in A memory (AMEM) and four in B memory (BMEM). Each FIFO has a block counter that counts the number of samples read or written by the IOC. It creates a dedicated interrupt signal, updates the block counter and updates the FIFO pointers when a new block has been read or written.

#### Memory Maps

The structure of the XMEM and YMEM address spaces are shown in Figure 5.





The structure of the PMEM address space is shown in Figure 6.

Figure 6. PMEM Memory Map

## OTHER DIGITAL BLOCKS AND FUNCTIONS

## General-Purpose Timer

The CFX DSP system contains two general purpose

## ANALOG BLOCKS

#### Input Stage

The analog audio input stage is comprised of four individual channels. For each channel, one input can be selected from any of the five possible input sources (depending on package option) and is then routed to the

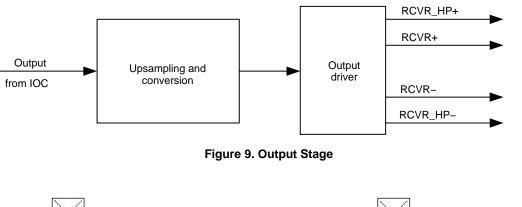
Channel 0

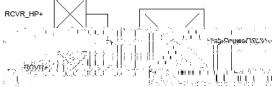
input of the programmable preamplifier that can be configured for bypass or gain values of 12 to 30 dB (3 dB steps). The input stage is shown in Figure 8.

A built in feature allows a sampling delay to be configured for any one or more channels. This is useful in beam forming applications.

Conversion and filtering

Figure 8. Input Stage





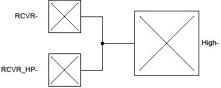
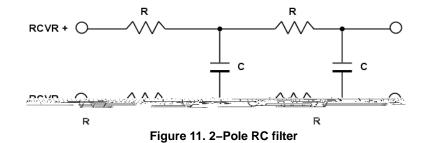


Figure 10. External Signal Routing of Connections for High–Power Output Mode

The high frequencies in the Class D PDM output are filtered by an RC filter or by the frequency response of the speaker itself. **onsemi** recommends a 2 pole RC filter on the

output stage if the output signal is not directly driving a receiver. Given below is the simple schematic for a 2 pole RC filter.



Our recommendations for components for the RC Filter are given below:

For 8 KHz sampling, we recommend R = 8.2 k and C = 1 nF (3 dB cutoff frequency at 3.3 kHz)

For 16 KHz sampling, we recommend R = 8.2 k and C = 330 pF (3 dB cutoff frequency at 9 kHz)

## **Clock Generation Circuitry**

BelaSigna 300 is equipped with an un calibrated internal RC oscillator that will provide clock support for booting and

stand by mode operations. This internal clocking circuitry cannot be used during normal operation; as such, an external clock signal must be present on the EXT\_CLK pin to allow BelaSigna 300 to operate. All other needed clocks in the system are derived from this external clock frequency. Figure 12 shows the internal clock structure of BelaSigna 300.



Figure 12. Internal Clocking Structure

## Power Supply Unit

BelaSigna 300 has multiple power sources as can be seen on Figure 13. Digital and analog sections of the chip have their own power supplies to allow exceptional audio quality.

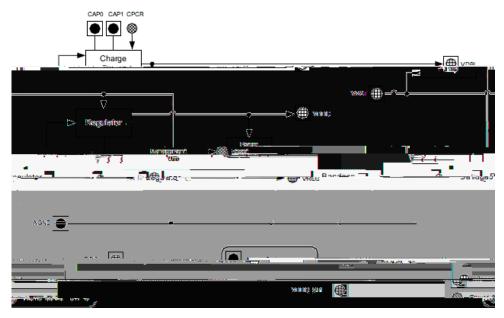


Figure 13. Power Supply Structure

## Battery Supply Voltage (VBAT)

The primary voltage supplied to a BelaSigna 300 device is VBAT. It is typically 1.8 V. BelaSigna 300 also uses VBAT to define the I/O voltage levels, as well as powering an external EEPROM on the SPI port. Consequently, any voltage below 1.8 V will result in incorrect operation of the EEPROM.

## Internal Band Gap Reference Voltage

The band gap reference voltage has been stabilized over temperature and process variations. This reference voltage is used in the generation of all of the regulated voltages in the BelaSigna 300 system and provides a nominal 1 V reference signal to all components using the reference voltage.

## Internal Digital Supply Voltage (VDDC)

The internal digital supply voltage is used as the supply voltage for all internal digital components, including being used as the interface voltage at the low side of the level translation circuitry attached to all of the external digital pads. VDDC is also provided as an output pad, where a capacitor to ground typically filters power supply noise. The VDDC internal regulator is a programmable power supply that allows the selection of the lowest digital supply depending on the clock frequency at which BelaSigna 300 will operate. In BelaSigna 300, the VDDC configuration is

## **APPLICATION DIAGRAMS**

The application diagram of BelaSigna 300 is shown in Figure 14.

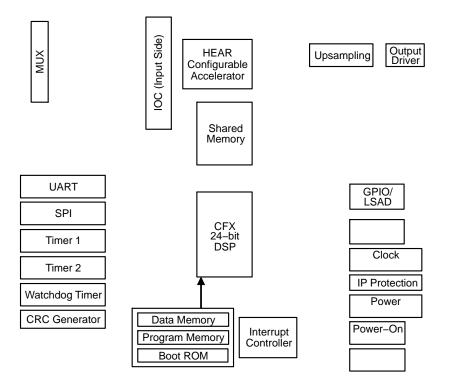


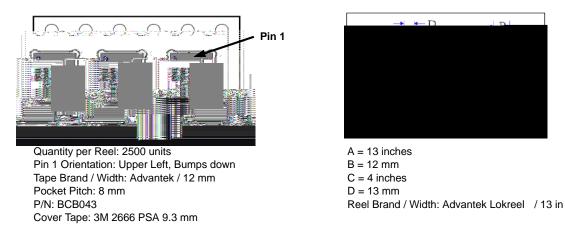
Figure 14. BelaSigna 300 Application Diagram

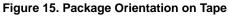
## **ASSEMBLY INFORMATION**

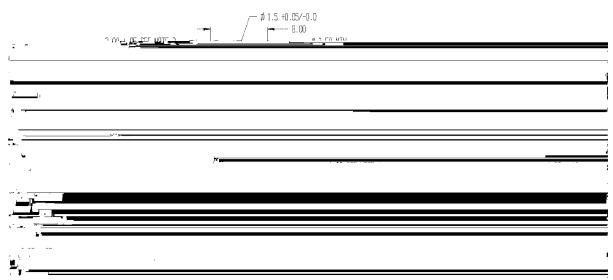
## CARRIER DETAILS

## 2.6 x 3.8 mm WLCSP

onsemi offers tape and reel packing for BelaSigna 300. The packing consists of a pocketed carrier tape, a cover tape, and a molded anti static polystyrene reel. The carrier and cover tape create an ESD safe environment, protecting the components from physical and electrostatic damage during shipping and handling.







10 sprockets hole pitch cumulative tolerance 0.1.

Camber in compliance with EIA 763.

Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

#### Figure 16. Carrier Tape Drawing

## **Re–Flow Information**

The re flow profile depends on the equipment that is used for the re flow and the assembly that is being re flowed. Information from JEDEC Standard 22 A113D and J STD 020D.01 can be used as a guideline.



DATE 20 OCT 2022

ASME Y14.5M, 1994.

CROWNS OF THE SOLDER BALLS.

0.244 0.269

3.63

RECOMMENDED Mounting footprint

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