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Integrated A/D Converters and Powered Output:

Flexible Clocking Architecture:

“Smart” Power Management:

Diverse Memory Architecture:

Data Security:

Development Tools:

Contents

FIGURES AND DATA

Table 1. ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Max	Unit
Voltage at any input pin	−0.3	2.0	V
Operating supply voltage (Note 1)	0.9	2.0	V
Operating temperature range (Note 2)	−40	8540	

Table 2. ELECTRICAL SPECIFICATIONS (continued)

Description	Symbol	Conditions	Min	Typ	Max	Units	Screened
VDBL (1 μF External Capacitor)							
Regulator PSRR	$VDBL_{PSRR}$	1 kHz	35	41	−	dB	
Load current	I_{LOAD}		−	−	2.5	mA	
Load regulation	$LOAD_{REG}$		−	7	10	mV/mA	
Line regulation	$LINE_{REG}$		−	10	20	mV/V	
VDDC (1 μF External Capacitor)							
Digital supply voltage output	VDDC	Configured by a control register	0.79	0.95	1.25	V	
VDDC output level adjustment	$VDDC_{STEP}$		27	29	31	mV	
Regulator PSRR	$VDDC_{PSRR}$	1 kHz	25	25.5	26	dB	
Load current	I_{LOAD}		−	−	3.5	mA	
Load regulation	$LOAD_{REG}$		−	3	12	mV/mA	
Line regulation	$LINE_{REG}$		−	3	8	mV/V	
POWER−							

WLCSP Pin Out

Assembly / Design Notes

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WLCSP Weight

Recommended Circuit Design Guidelines

Recommended Ground Design Strategy

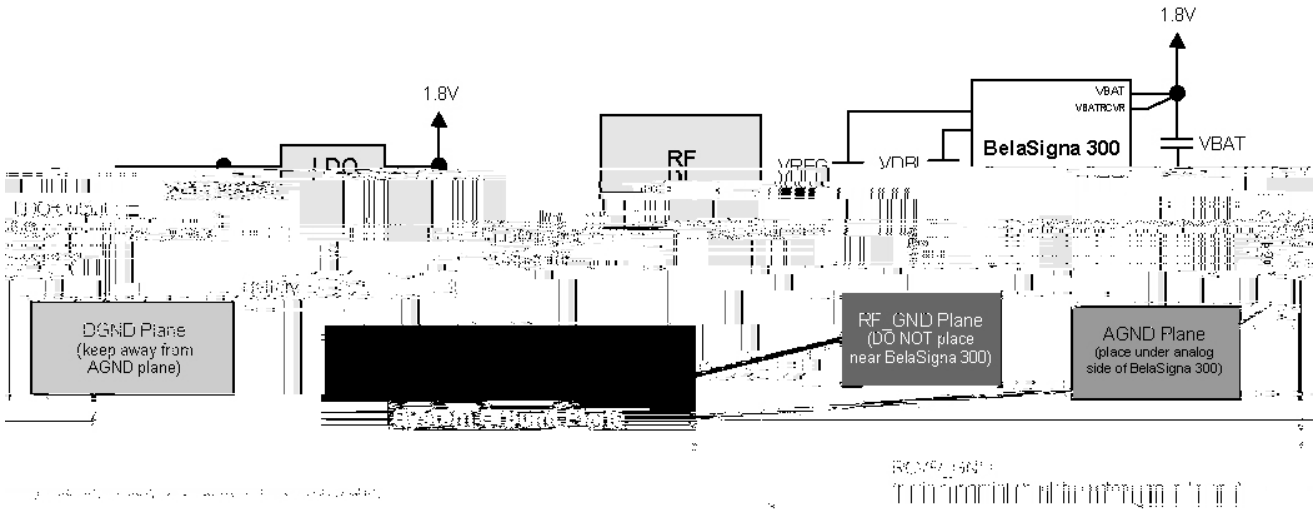

Figure 1. Schematic of Ground Scheme

Table 7. NON−CRITICAL SIGNALS

Pin Name	Description	Routing Guideline
CAP0, CAP1	Internal charge pump − capacitor connection	Place 100 nF capacitor close to pins
SDA, SCL	I2C port	Keep as short as possible
GPIO[3..0]	General−purpose I/O	Not critical
UART_RX, UART_TX	General−purpose UART	Not critical
PCM_FRAME, PCM_CLK, PCM_OUT, PCM_IN	PCM port	Keep away from analog input lines
LSAD[4..1]	Low−speed A/D converters	Not critical
SPI_CLK, SPI_CS, SPI_SERI, SPI_SERO	Serial peripheral interface port Connect to EEPROM	Keep away from analog input lines

Audio Inputs

Ω

Audio Outputs

Recommendation for Unused Pins

Table 8. RECOMMENDATIONS FOR UNUSED PADS

WLCSP Ball Index	BelaSigna 300 Signal Name	Recommended Connection when Not Used
B2	RCVR_HP+	Do not connect
C3	RCVR+	Do not connect
A3	RCVR−	Do not connect
B4	RCVR_HP−	Do not connect
A11	AI4	Connect to AGND
N/A	AI3/LOUT3	Connect to AGND
B12	AI2/LOUT2	Connect to AGND
A13	AI1/LOUT1	Connect to AGND
B14	AI0/LOUT0	Connect to AGND
D14	GPIO[4]/LSAD[4]	

Table 8. RECOMMENDATIONS FOR UNUSED PADS (continued)

WLCSP Ball Index	BelaSigna 300 Signal Name	Recommended Connection when Not Used
D6	SPI_CS	

CFX DSP Core

CFX DSP Architecture

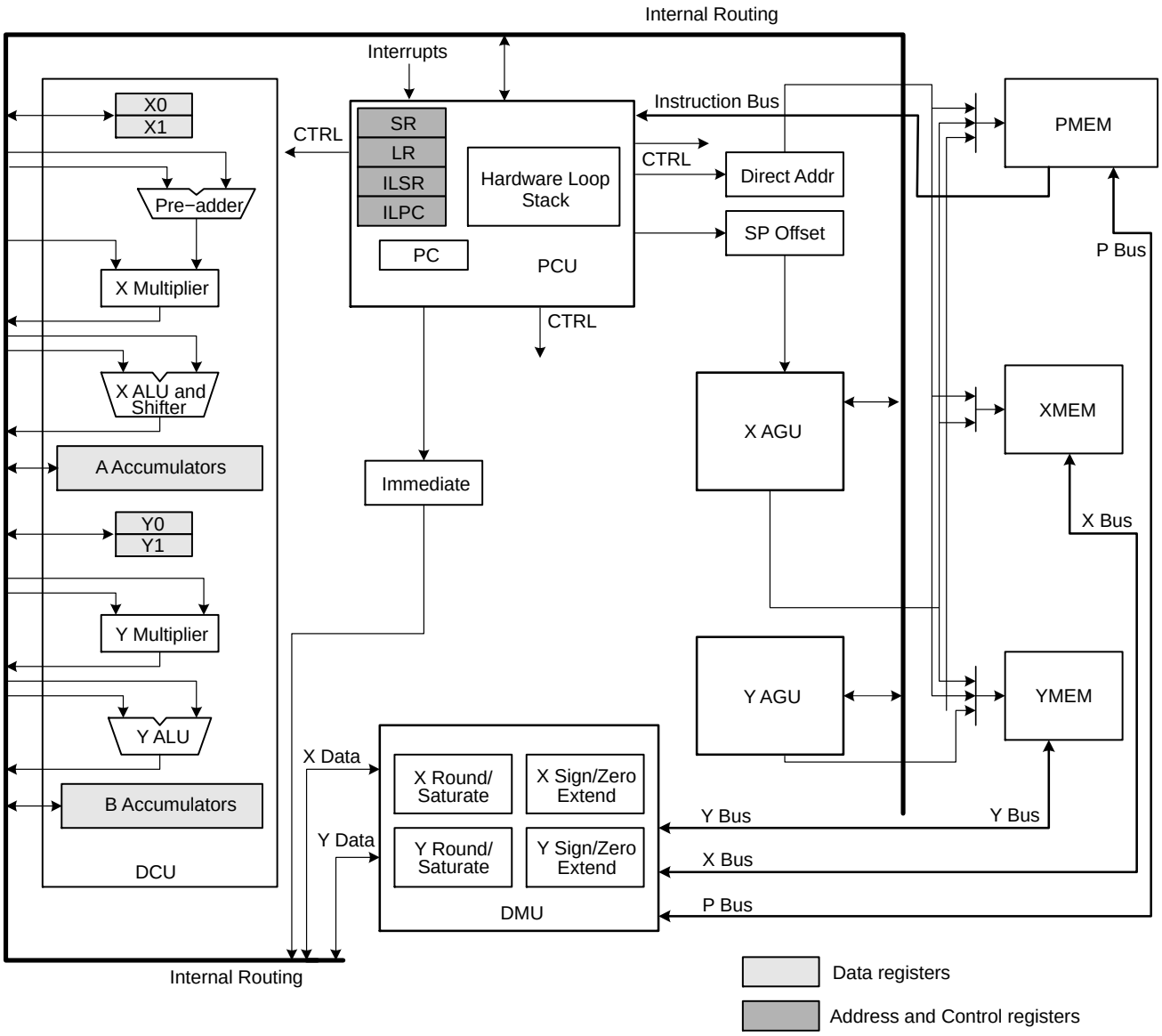

Figure 3. CFX DSP Core Architecture

CFX DSP Instruction Set

Table 9. CFX SUMMARY INSTRUCTION SET

Instruction	Description
ABS	Calculate the absolute value of a data register or accumulator
ADD	

Table 9. CFX SUMMARY INSTRUCTION SET (continued)

Instruction	Description
RETURN	Return from a subroutine
RETURNI	Return from an interrupt
SHLL	Shift a data register left logically
SHRA	Shift a data register right arithmetically
SHRL	Shift a data register right logically
SLEEP	Enter sleep mode and wait for an interrupt and then wake up from sleep mode
STORE	Store data, a register or accumulator in a register, accumulator or memory location
SUB	Subtract two data registers or accumulators, storing the result in a data register or accumulator
SUBMUL	Subtract two XY data registers, multiply the result by a third XY data register, and store the result in an accumulator
SUBMULADD	Subtract two XY data registers, multiply the result by a third XY data register, and add the result to an accumulator
SUBMULNEG	Subtract two XY data registers, multiply the result by a third XY data register, negate the result and store it in an accumulator
SUBMULSUB	Subtract two XY data registers, multiply the result by a third XY data register, and subtract the result from an accumulator
SUBSH	Subtract two data registers or two accumulators and shift right one bit, storing the result in a data register or accumulator
SUBSTEP	Subtract a step register from the corresponding pointer
SWAP	Swap the contents of two data registers, conditionally
XOR	Perform a bitwise XOR operation on two data registers or a data register and a value, storing the result in a data register

HEAR Configurable Accelerator

Shared Memories

Table 11. SHARED MEMORIES

Type	Name	Size
Data memory (RAM)	H0MEM, H1MEM, H2MEM, H3MEM, H4MEM, H5MEM	Each 128x48−bit words
FIFO memory (RAM)	AMEM, BMEM	Each 1024x48−bit words
Coefficient memory (RAM)	CMEM, DMEM	Each 1024x48−bit words
Data ROM	SIN/COS LUT	512x48−bit words containing the 512 point sin/cos look up table
Microcode memory (RAM)	MICROCODE_MEM	2048x32−bit words

Memories Structure

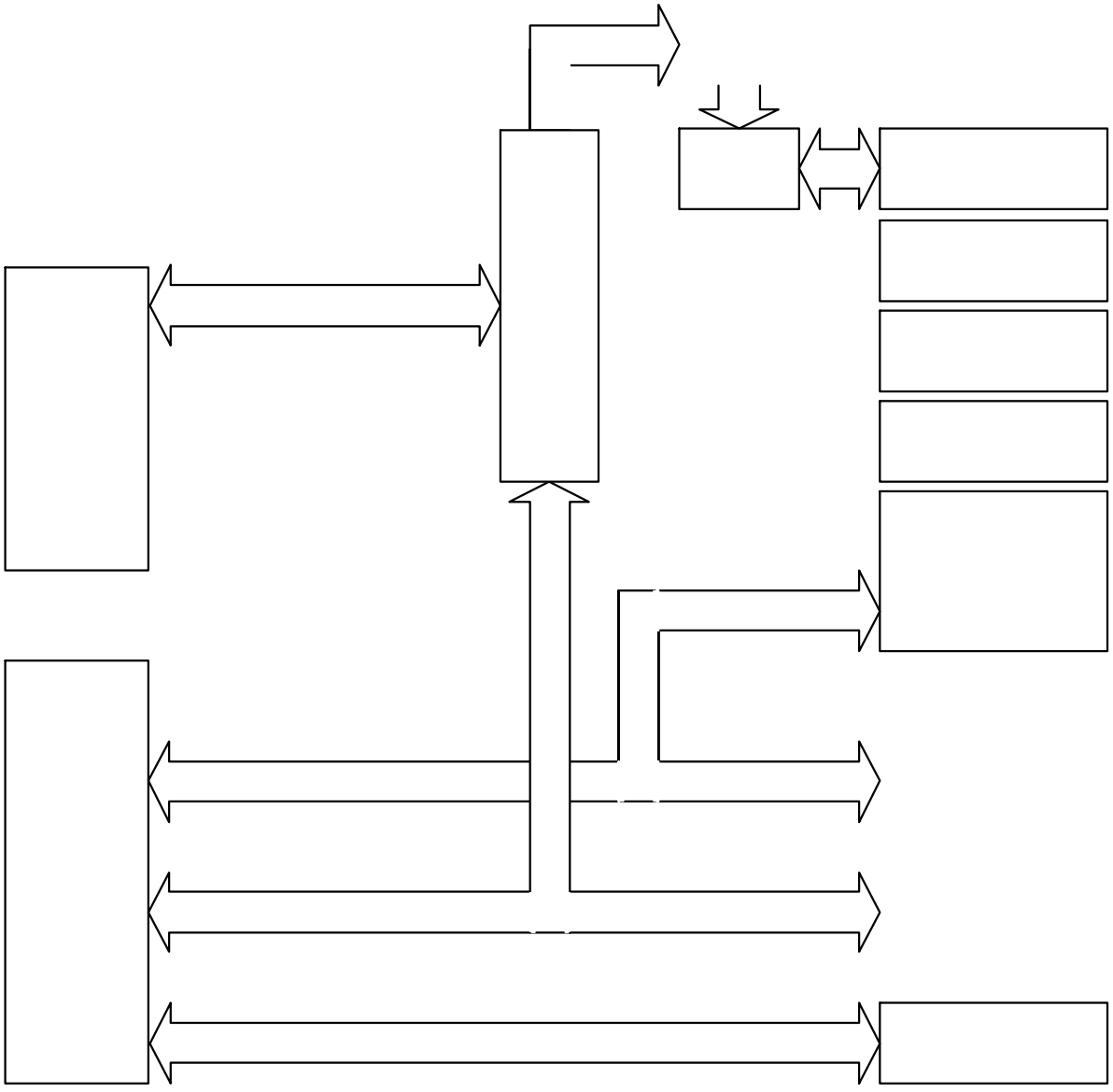

Figure 4. System Memory Architecture

FIFO Controller

Memory Maps

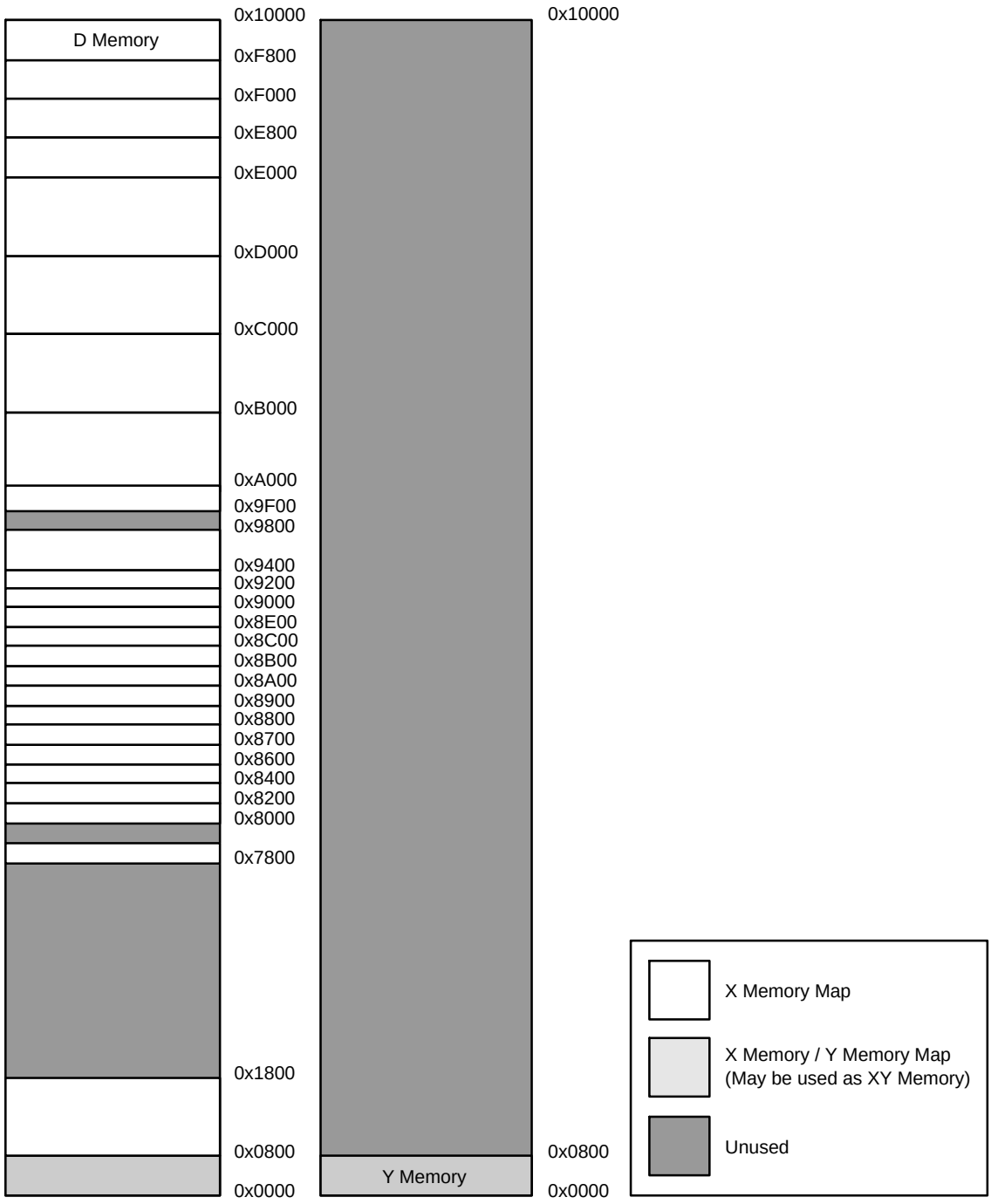

Figure 5. XMEM and YMEM Memory Maps

Figure 6. PMEM Memory Map

OTHER DIGITAL BLOCKS AND FUNCTIONS

General−Purpose Timer

ANALOG BLOCKS

Input Stage

Figure 8. Input Stage

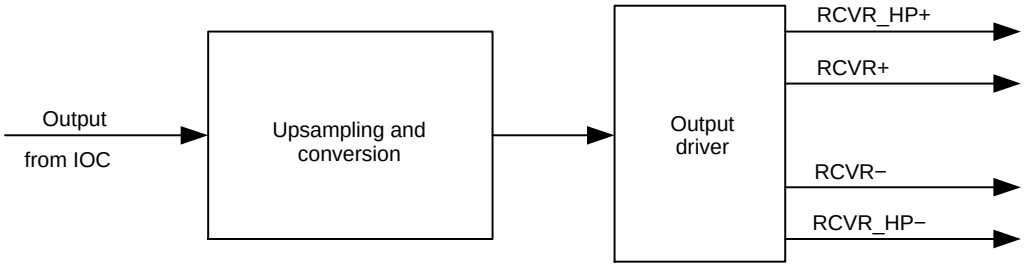

Figure 9. Output Stage

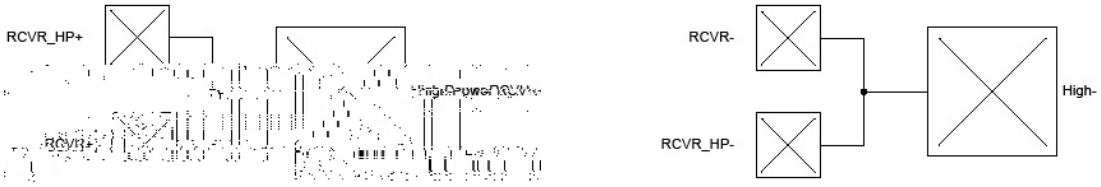

Figure 10. External Signal Routing of Connections for High−Power Output Mode

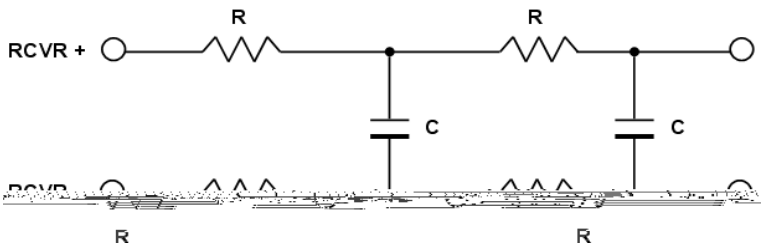

Figure 11. 2−Pole RC filter

Clock Generation Circuitry

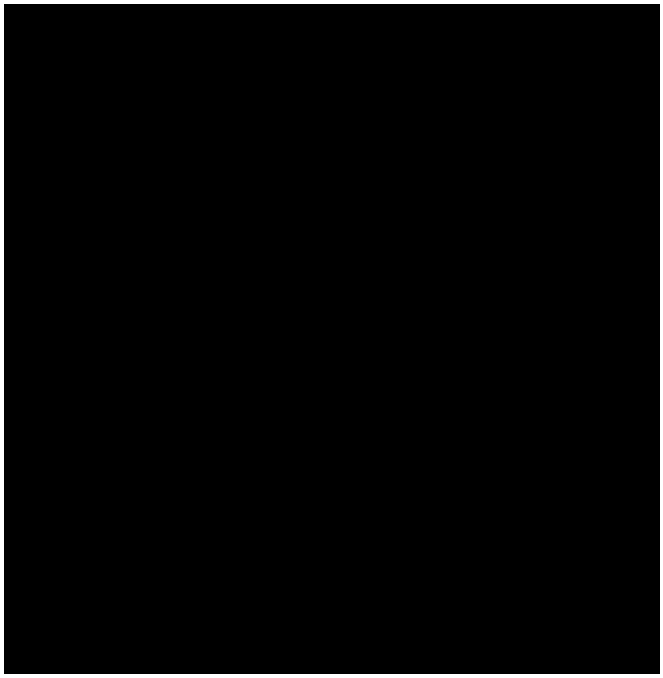

Figure 12. Internal Clocking Structure

Power Supply Unit

Figure 13. Power Supply Structure

Battery Supply Voltage (VBAT)

Internal Band Gap Reference Voltage

Internal Digital Supply Voltage (VDDC)

APPLICATION DIAGRAMS

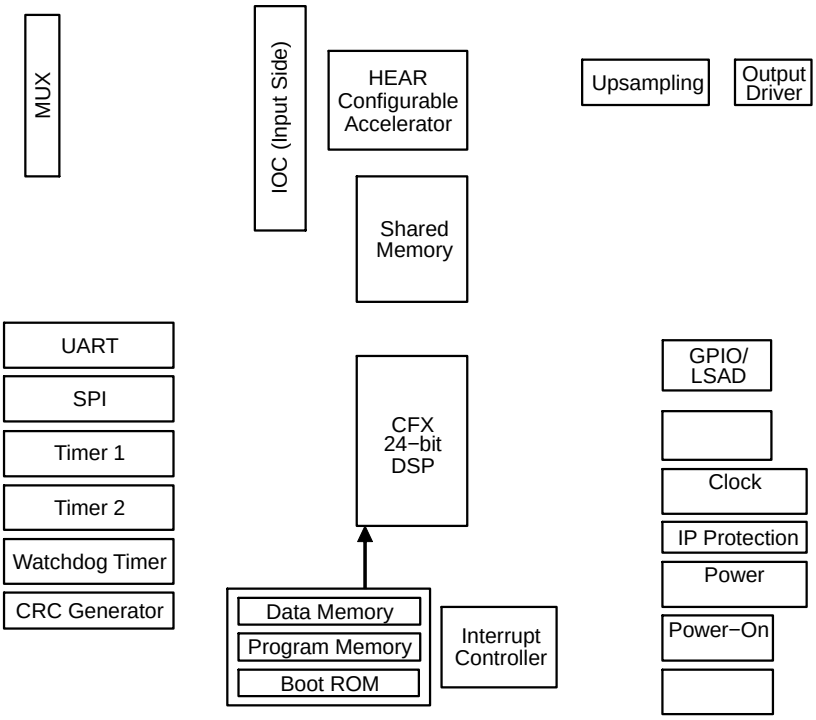

Figure 14. BelaSigna 300 Application Diagram

ASSEMBLY INFORMATION

CARRIER DETAILS
2.6 x 3.8 mm WLCSP
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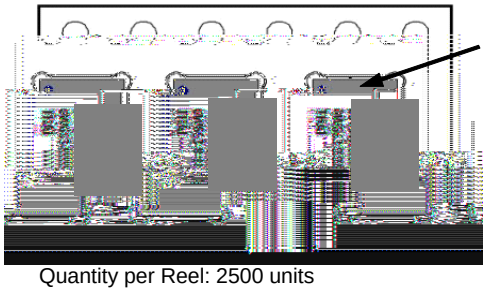
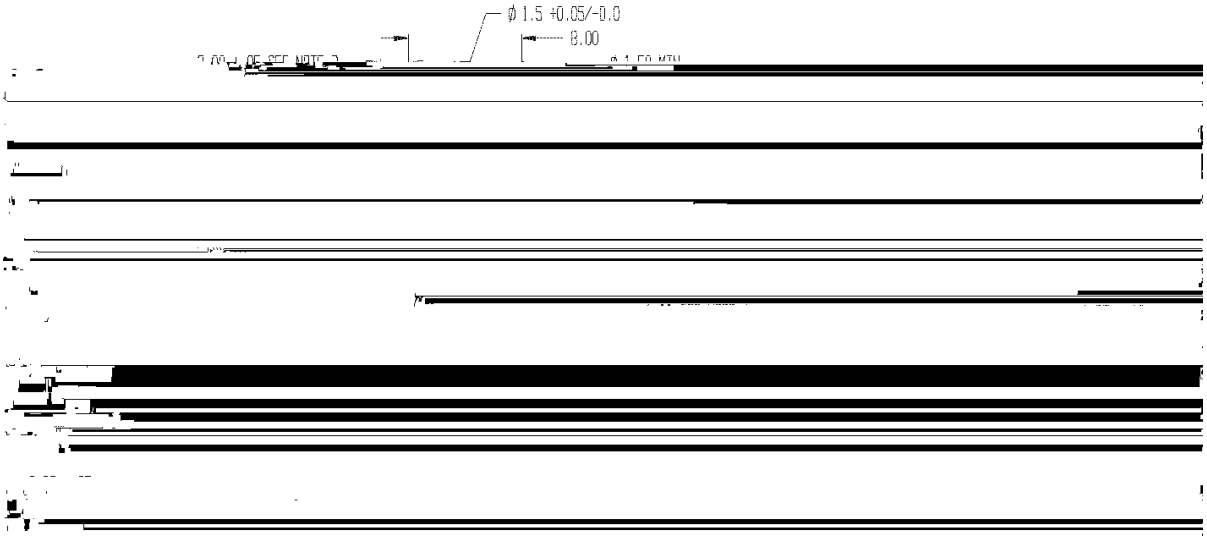


Quantity per Reel: 2500 units
Pin 1 Orientation: Upper Left, Bumps down
Tape Brand / Width: Advantek / 12 mm
Pocket Pitch: 8 mm
P/N: BCB043
Cover Tape: 3M 2666 PSA 9.3 mm

A = 13 inches
B = 12 mm
C = 4 inches
D = 13 mm
Reel Brand / Width: Advantek Lokreel / 13 in

Figure 15. Package Orientation on Tape



10 sprockets hole pitch cumulative tolerance 0.1.
Camber in compliance with EIA 763.
Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

Figure 16. Carrier Tape Drawing

Re−Flow Information

WLCSP35, 3.63x2.68
CASE 567AG
ISSUE C

DATE 20 OCT 2022

ASME Y14.5M, 1994.

CROWNS OF THE SOLDER BALLS.

0.244 0.269

3.63

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