# AX-SFUS, AX-SFUS-API

# Ultra-Low Power, AT Command / API Controlled, Sigfox® Compliant Transceiver IC for Up-Link and Down-Link

## OVERVIEW

### Circuit Description

AX−SFUS and AX−SFUS−API are ultra−low power single chip solutions for a node on the Sigfox network with both up− and down−link functionality. The AX−SFUS chip is delivered fully ready for operation and contains all the necessary firmware to transmit and receive data from the Sigfox network in the US (SIGFOX RCZ2 region). It connects to the customer product using a logic level RS232 UART. AT commands are used to send frames and configure radio parameters.

The AX−SFUS−API variant is intended for customers wishing to write their own application software based on the AX−SF−LIB−1−GEVK library.

### Features

Functionality and Ecosystem

- Sigfox up−link and down−link functionality controlled by AT commands or API
- The AX−SFUS and AX−SF−API ICs are part of a whole development and product ecosystem available from ON Semiconductor for any Sigfox requirement. Other parts of the ecosystem include
  - Ready to go development kit DVK−SFEU−[API]−1−GEVK including a 2 year Sigfox subscription
  - Sigfox Ready® certified reference design for the AX−SFUS and AX−SFUS−API ICs

General Features

- QFN40 5 mm x 7 mm package
- Supply range 2.7 V* − 3.6 V
- −40°C to 85°C
- Temperature sensor
- Supply voltage measurements

*Includes the RF frontend module, circuit as in Figure 5. The AX−SFUS chip alone is operational from 1.8 V to 3.6 V, a supply



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## BLOCK DIAGRAM

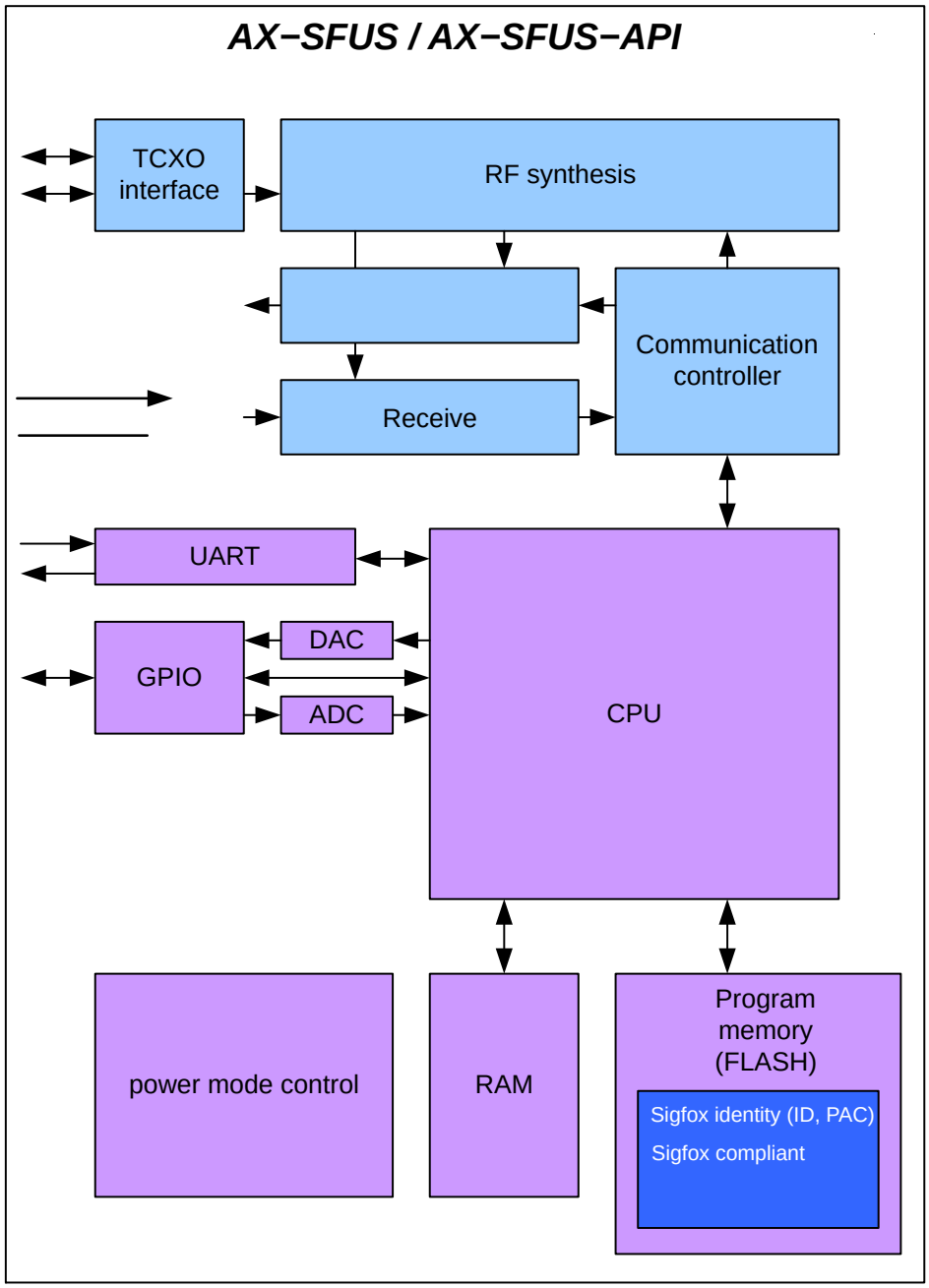



**Figure 1. Functional Block Diagram of the AX−SFUS / AX−SFUS−API**

**Table 1. PIN FUNCTION DESCRIPTIONS**

| Symbol | Pin(s) | Type | Description |
|---|---|---|---|
| VDD_ANA | 1 | P | Analog power output, decouple to neighboring GND |
| GND | 2 | P | Ground, decouple to neighboring VDD_ANA |
| ANTP | 3 | A | Differential receive input |
| ANTN | 4 | A | Differential receive input |
| ANTP1 | 5 | N | Single ended transmit output |
| GND | 6 | P | Ground, decouple to neighboring VDD_ANA |
| VDD_ANA | 7 | P | Analog power output, decouple to neighboring GND |
| GND | 8 | P | Ground |
| FILT | 9 | A | Synthesizer filter |
| L2 | 10 | A | Must be connected to pin L1 |
| L1 | 11 | A | Must be connected to pin L2 |
| NC | 12 | N | Do not connect |
| GPIO8 | 13 | I/O/PU | General purpose IO |
| GPIO7 | 14 | I/O/PU | General purpose IO, selectable SPI functionality (MISO) |
| GPIO6 | 15 | I/O/PU | General purpose IO, selectable SPI functionality (MOSI) |
| GPIO5 | 16 | I/O/PU | General purpose IO, selectable SPI functionality (SCK) |
| GPIO4 | 17 | I/O/PU | General purpose IO, selectable ΣΔ DAC functionality, selectable dock functionality |
| CPU_LED | 18 | O | CPU activity indicator |
| RADIO_LED | 19 | O | Radio activity indicator |
| VTCXO | 20 | O | TCXO power |
| GPIO9 | 21 | I/O/PU | General purpose IO, wakeup from deep sleep |
| UARTTX | 22 | O | UART transmit |
| UARTRX | 23 | I/PU | UART receive |
| RX_LED | 24 | O | Receive activity indicator |
| TX_LED | 25 | O | Transmit activity indicator |
| NC | 26 | PD | Do not connect |
| RESET_N | 27 | I/PU | Optional reset pin. Internal pull−up resistor is permanently enabled, nevesref200.466he 298.602 .6803 ref 435.4582r1200.466 298.035 .68033 2istor is permane 298.60 |

# AX-SFUS, AX-SFUS-API

## SPECIFICATIONS

**Table 3. ABSOLUTE MAXIMUM RATINGS**

| Symbol | Description | Condition | Min | Max | Units |
|---|---|---|---|---|---|
| VDD_IO | Supply voltage | | −0.5 | 5.5 | V |
| | | | | 200 | mA |

## DC Characteristics

### Table 4. SUPPLIES

Conditions for all current and charge values unless otherwise specified are for the hardware configuration described in the AX−SFUS Application Note: Sigfox Compliant Reference Design.

| Symbol | Description | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $T_{AMB}$ | Operational ambient temperature | | −40 | 27 | 85 | °C |
| $VDD_{IO}$ | I/O and voltage regulator supply voltage AX−SFUS chip only | | 1.8* | 3.0 | 3.6 | V |
| $VDD_{IO\_mod}$ | I/O and voltage regulator supply voltage AX−SFUS with RF frontend module as in Figure 5 | | 2.7 | 3.3 | 3.6 | V |
| $VDD_{IO\_R1}$ | I/O voltage ramp for reset activation; Note 1 | Ramp starts at VDD_IO ≤ 0.1 V | 0.1 | | | V/ms |
| $VDD_{IO\_R2}$ | I/O voltage ramp for reset activation; Note 1 | Ramp starts at 0.1 V < VDD_IO < 0.7 V | 3.3 | | | V/ms |
| $I_{DS}$ | Deep sleep mode current; Note 3 | AT$P=2 | | 350 | | nA |
| $I_{SLP}$ | Sleep mode current; Note 3 | AT$P=1 | | 1.6 | | μA |
| $I_{STDBY}$ | Standby mode current Notes 2, 3 | | | 0.5 | | mA |
| $I_{RX\_CONT}$ | Current consumption continuous RX; Note 3 | AT$TM=3,255 | | 34 | | mA |
| $Q_{SFX\_OOB\_24}$ | Charge to send a Sigfox out of band message, 24 dBm; Note 3 | AT$S0 | | 0.25 | | C |
| $Q_{SFX\_BIT\_24}$ | Charge to send a bit, 24 dBm; Note 3 | AT$SB=0 | | 0.22 | | C |
| $Q_{SFX\_BITDL\_24}$ | Charge to send a bit with downlink receive, 24 dBm; Note 3 | AT$SB=0,1 | | 0.28 | | C |
| $Q_{SFX\_LFR\_24}$ | Charge to send the longest possible Sigfox frame (12 byte) , 24 dBm; Note 3 | AT$SF=00112233445566778899aabb | | 0.73 | | C |
| $Q_{SFX\_LFRDL\_24}$ | Charge to send the longest possible receive, 24 dBm; Note 3 refBT8 0 0 T74.78LFRDL_266eu453.619 ref457.625 666.652 29.877 .9071 refBT8 0 0 8fossible rec945 51s0SETdn8T74.e longest possible | | | | | |

**Typical Current Waveform**

**Table 5. LOGIC**

| Symbol | Description | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Digital Inputs** | | | | | | |
| $V_{T+}$ | Schmitt trigger low to high threshold point | VDD_IO = 3.3 V | | 1.55 | | V |
| $V_{T−}$ | Schmitt trigger high to low threshold point | | | 1.25 | | V |
| $V_{IL}$ | Input voltage, low | | | | 0.8 | V |
| $V_{IH}$ | Input voltage, high | | 2.0 | | | V |
| $V_{IPA}$ | Input voltage range, GPIO[3:0] | | −0.5 | | VDD_IO | V |
| $V_{IPBC}$ | Input voltage range, GPIO[9:4], UARTRX | | −0.5 | | 5.5 | V |
| $I_L$ | Input leakage current | | −10 | | 10 | μA |
| $R_{PU}$ | Programmable Pull−Up Resistance | | | 65 | | kΩ |
| **Digital Outputs** | | | | | | |
| $I_{OH}$ | Output Current, high<br>Ports GPIO[9:0], UARTTX, TXLED, RXLED, TXLED, CPULED | $V_{OH}$ = 2.4 V | 8 | | | mA |
| $I_{OL}$ | Output Current, low<br>GPIO[9:0], UARTTX, TXLED, RXLED, TXLED, CPULED | $V_{OL}$ = 0.4 V | 8 | | | mA |
| $I_{OZ}$ | Tri−state output leakage current | | −10 | | 10 | μA |

## AC Characteristics

**Table 6. TCXO REFERENCE INPUT**

| Symbol | Description | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $f_{TCXO}$ | TCXO frequency | A passive network between the TCXO output and the pins CLKP and CLKN is required.<br>For detailed TCXO network recommendations depending on the TCXO output swing refer to | | | | |

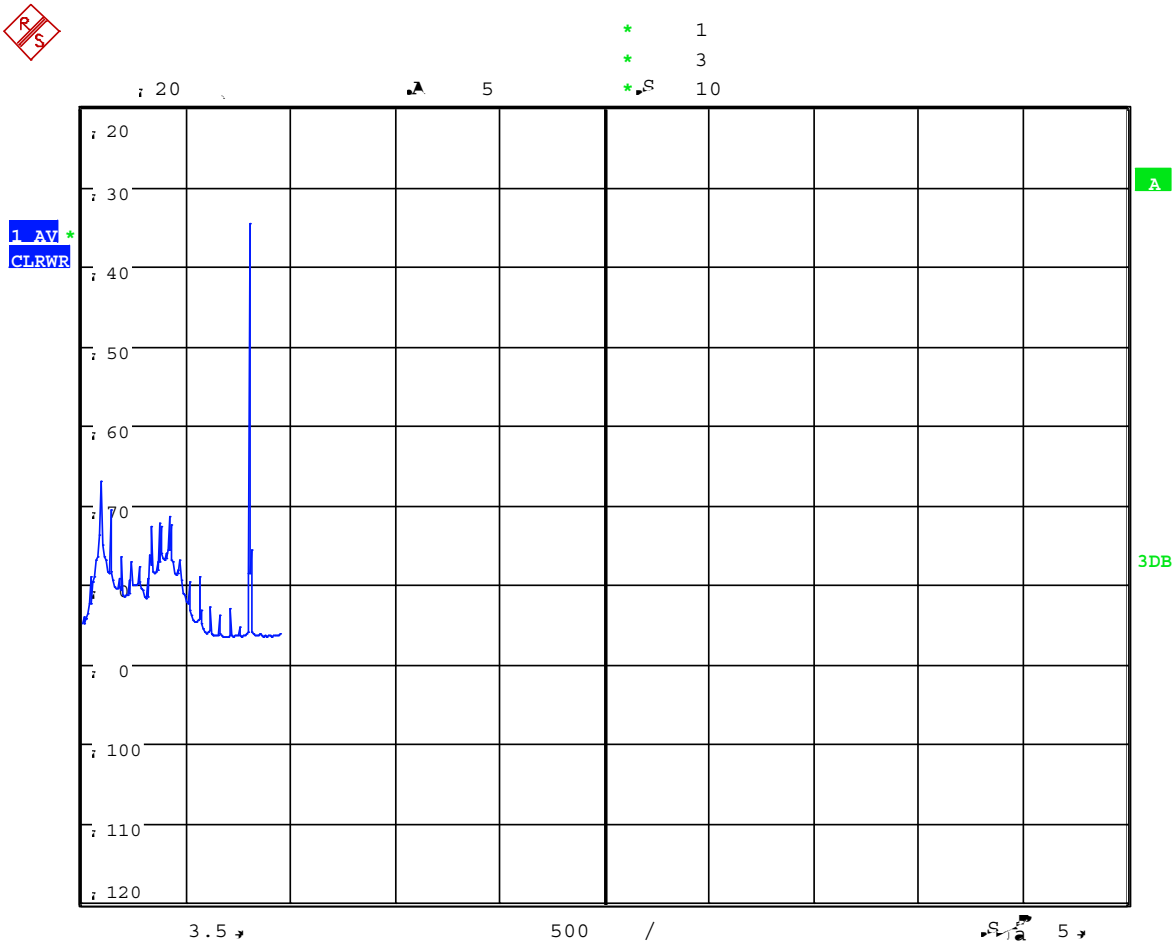



**Figure 4. Typical Spectrum with Harmonics at 24 dBm Output Power**

**Table 9. ADC / TEMPERATURE SENSOR**

| Symbol | Description | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| ADCRES | ADC resolution | | | 10 | | Bits |
| $V_{ADCREF}$ | ADC reference voltage | | 0.95 | 1 | 1.05 | V |
| $Z_{ADC00}$ | Input capacitance | | | | 2.5 | pF |
| DNL | Differential nonlinearity | | | ± 1 | | LSB |
| INL | Integral nonlinearity | | | ± 1 | | LSB |
| OFF | | | | | | |

**AT$CB=0011223344,1**
OK
RX=AA BB CC DD

This sends a Sigfox frame containing { 0xAA : 0xBB : 0x12 : 0x34 } without waiting for a response telegram.

**AT$CB=0xAA,1**
OK

The ‘CB’ command sends out a continuous pattern of bits, in this case 0xAA = 0b10101010.

**AT$P=1**
OK

This transitions the device into sleep mode. Out−of−band transmissions will

**Table 10. COMMANDS**

| Command | Name | Description |
|---|---|---|
| AT$V? | Get Voltages | Return current voltage and voltage measured during the last transmission in mV. |
| AT$I=uint | Information | Display various product information:<br>0: Software Name & Version<br>Example Response: AX−Sigfox 1.1.1−FCC<br>1: Contact Details<br>Example Response: support@axsem.com<br>2: Silicon revision lower byte<br>Example Response: 8F<br>3: Silicon revision upper byte<br>Example Response: 51<br>4: Major Firmware Version<br>Example Response: 1<br>5: Minor Firmware Version<br>Example Response: 1<br>7: Firmware Variant (Frequency Band etc. (EU/US))<br>Example Response: FCC<br>9: SIGFOX Library Version<br>Example Response: UDL1−1.8.7<br>10: Device ID<br>Example Response: 00012345<br>11: PAC<br>Example Response: 0123456789ABCDEF |
| AT$P=uint | Set Power Mode | To conserve power, the AX−SFUS can be put to sleep manually. Depending on power mode, you will be responsible for waking up the AX−SFUS again!<br>0: software reset (settings will be reset to values in flash)<br>1: sleep (send a break to wake up)<br>2: deep sleep (toggle GPIO9 or RESET_N pin to wake up; the AX−SFUS is not running and all settings will be reset!) |
| AT$WR | Save Config | Write all settings to flash (RX/TX frequencies, registers) so they survive reset/deep sleep or loss of power.<br>Use AT$P=0 to reset the AX−SFUS and load settings from flash. |
| AT:Pn? | Get GPIO Pin | Return the setting of the GPIO Pin *n*; *n* can range from 0 to 9. A character string is returned describing the mode of the pin, followed by the actual value. If the pin is configured as analog pin, then the voltage (range 0…1 V) is returned. The mode characters have the following meaning:<br>**Mode** **Description**<br>0 Pin drives low<br>1 Pin drives high<br>Z Pin is high impedance input<br>U Pin is input with pull−up |

**Table 10. COMMANDS**

| Command | Name | Description |
|---|---|---|
| AT:ADC Pn[−Pn[ (1V\|10V)]]? | Get GPIO Pin Analog Voltage | Measure the voltage applied to a GPIO pin. The command also allows measurement of the voltage difference across two GPIO pins. In differential mode, the full scale range may also be specified as 1 V or 10 V. Note however that the pin input voltages must not exceed the range 0..VDD_IO. The command returns the result as fraction of the full scale range (1 V if none is specified). The GPIO pins referenced should be initialized to analog mode before issuing this command. |
| AT:SPI[(A\|B\|C\|D)]=bytes | SPI Transaction | This command clocks out *bytes* on the SPI port. The clock frequency is 312.5 kHz. The command returns the bytes read on MISO during output. Optionally the clocking mode may be specified (default is A):<br><br>**Mode** / **Clock Inversion** / **Clock Phase**<br>A / normal / normal<br>B / normal / alternate<br>C / inverted / normal<br>D / inverted / alternate<br><br>D7 … D |

**Table 10. COMMANDS**

| Command | Name | Description |
|---|---|---|
| AT$TM=mode,config | Activates the Sigfox Testmode | Available test modes:<br>0. TX BPSK<br>Send only BPSK with Synchro Bit + Synchro frame + PN sequence: No hopping centered on the TX_frequency. Config bits 0 to 6 define the number of repetitions. Bit 7 of config defines if a delay is applied of not in the loop<br>1. TX Protocol:<br>Tx mode with full protocol with Sigfox key: Send Sigfox protocol frames with initiate downlink flag = True. Config defines the number of repetitions.<br>2. RX Protocol:<br>This mode tests the complete downlink protocol in Downlink only. Config defines the number of repetitions.<br>3. RX GFSK:<br>RX mode with known pattern with SB + SF + Pattern on RX_frequency (internal comparison with received frame ⇔ known pattern = AA AA B2 27 1F 20 41 84 32 68 C5 BA AE 79 E7 F6 DD 9B. Config defines the number of repetitions. Config defines the number of repetitions.<br>4. RX Sensitivity:<br>Does uplink + downlink frame with Sigfox key and specific timings. This test is specific to SIGFOX's test equipments & softwares.<br>5. TX Synthesis:<br>Does one uplink frame on each Sigfox channel to measure frequency synthesis step |
| AT$SE | Starts AT$TM−3,255 indefinitely | Convenience command for sensitivity tests |
| AT$SL[=frame] | Send local loop | Sends a local loop frame with optional payload of 1 to 12 bytes. Default payload: 0x84, 0x32, 0x68, 0xC5, 0xBA, 0x53, 0xAE, 0x79, 0xE7, 0xF6, 0xDD, 0x9B. |
| AT$RL | Receive local loop | Starts listening for a local loop. |

**Table 11. REGISTERS**

| Number | Name | Description | Default | Range | Units |
|---|---|---|---|---|---|
| 300 | Out Of Band Period | AX−SFUS sends periodic static messages to indicate that they are alive. Set to 0 to disable. | 24 | 0−24 | hours |
| 400 | Macrochannel Mask | The mask of Macrochannels to use. | <000001FF><br><00000000><br><00000000>,1 | | |
| 410 | Encryption Key Configuration | Set to zero for normal operation. Set to one for use with the SIGFOX Network Emulator Kit (SNEK) | 0 | 0−1 | 0: private key<br>1: public key |

## APPLICATION INFORMATION

### Typical Application Diagrams

*Typical AX−SFUS / AX−SFUS−API Application Diagram*

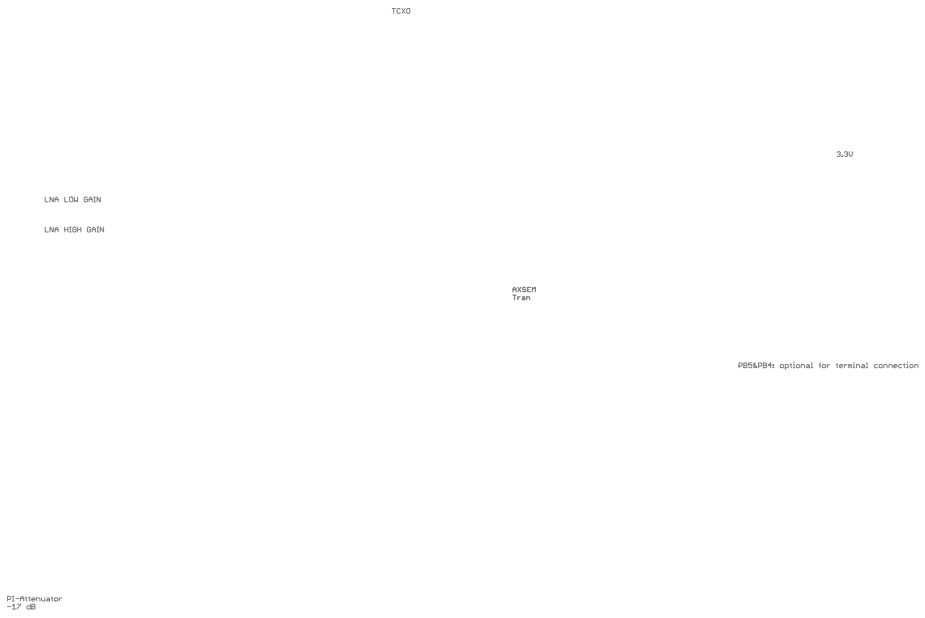
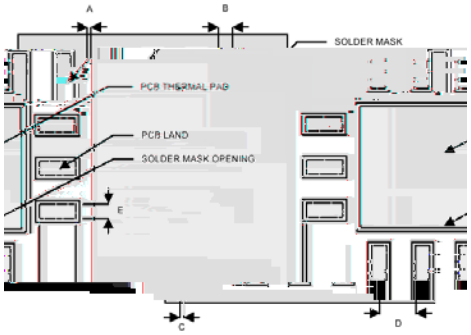



**Figure 5. Typical Application Diagram**

### QFN40 Recommended Pad Layout

1. PCB land and solder masking recommendations are shown in Figure 7.




A = Clearance from PCB thermal pad to solder mask opening, 0.0635 mm minimum
B = Clearance from edge of PCB thermal pad to PCB land, 0.2 mm minimum
C = Clearance from PCB land edge to solder mask opening to be as tight as possible to ensure that some solder mask remains between PCB pads.
D = PCB land length = QFN solder pad length + 0.1 mm
E = PCB land width = QFN solder pad width + 0.1 mm

**Figure 7. PCB Land and Solder Mask Recommendations**

2. Thermal vias should be used on the PCB thermal pad (middle ground pad) to improve thermal conductivity from the device to a copper ground plane area on the reverse side of the printed circuit board. The number of vias depends on the package thermal requirements, as determined by thermal simulation or actual testing.
3. Increasing the number of vias through the printed circuit board will improve the thermal conductivity to the reverse side ground plane and external heat sink. In general, adding more metal through the PC board under the IC will improve operational heat transfer, but will require careful attention to uniform heating of the board during assembly.

### Assembly Process

*Stencil Design & Solder Paste Application*

1. Stainless steel stencils are recommended for solder paste application.
2. A stencil thickness of 0.125 – 0.150 mm (5 – 6 mils) is recommended for screening.
3. For the PCB thermal pad, solder paste should be printed on the PCB by designing a stencil with an array of smaller openings that sum to 50% of the QFN exposed pad area. Solder paste should be applied through an array of squares (or circles) as shown in Figure 8.
4. The aperture opening for the signal pads should be between 50−80% of the QFN pad area as shown in Figure 9.
5. Optionally, for better solder paste release, the aperture walls should be trapezoidal and the corners rounded.
6. The fine pitch of the IC leads requires accurate alignment of the stencil and the printed circuit board. The stencil and printed circuit assembly should be aligned to within + 1 mil prior to

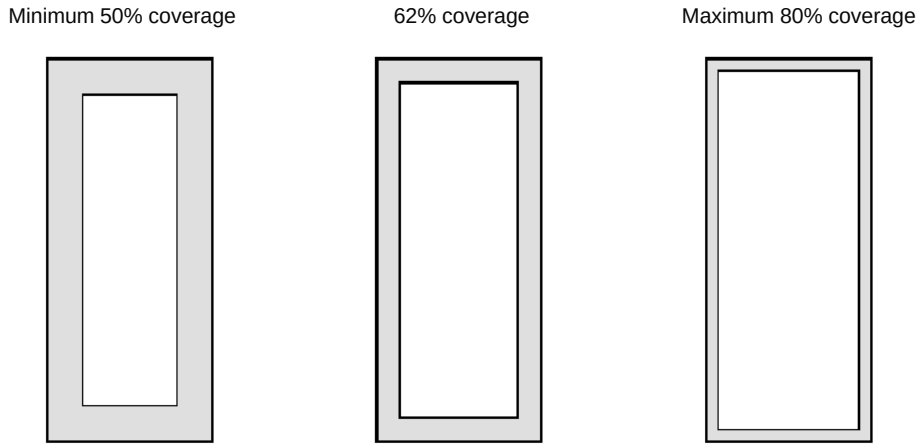



**Figure 9. Solder Paste Application on Pins**

### Life Support Applications

This product is not designed for use in life support appliances, devices, or in systems where malfunction of this product can reasonably be expected to result in personal injury. ON Semiconductor customers using or selling this product for use in such applications do so at their own risk and agree to fully indemnify ON Semiconductor for any damages resulting from such improper use or sale.

### Device Information

The following device information can be queried using the AT−Commands AT$I=4, AT$I=5 for the APP version and AT$I=2, AT$I=3 for the chip version.

**Table 13. DEVICE VERSIONS**

| Product | Part Number | APP Version | | Chip Version | |
|---|---|---|---|---|---|
| | | [0] | [1] | [0] | [1] |
| AX−SFUS | AX−SFUS−1−01−XXXX[1] | 0x01 | 0x01 | 0x8F | 0x51 |
| AX−SFUS−API | AX−SFUS−API−1−01−XXXX[1] | 0x01 | 0x01 | 0x8F | 0x51 |

1. TB05 for Reel 500, TX30 for Reel 3000 reel

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30mm FROM TERMINAL
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| | | |
|---|---|---|
| | | |
| | 0.80 | 1.00 |
| | 0.00 | 0.05 |
| | 0.20 REF | |
| | 0.18 | 0.300 |

0.05b