AMIS-42770

Dual High Speed CAN Transceiver

General Description

Controller Area Network (CAN) is a serial communication protocol, which supports distributed real−time control and multiplexing with high safety level. Typical applications of CAN−based networks can be found in automotive and industrial environments.

The AMIS−42770 Dual−CAN transceiver is the interface between up to two physical bus lines and the protocol controller and will be used for serial data interchange between different electronic units at more than one bus line. It can be used for both 12 V and 24 V systems.

The circuit consists of following blocks:

- Two differential line transmitters
- Two differential line receivers
- Interface to the CAN protocol handler
- Interface to expand the number of CAN busses
- Logic block including repeater function and the feedback suppression
- Thermal shutdown circuit (TSD)

Due to the wide common−mode voltage range of the receiver inputs, the AMIS−42770 is able to reach outstanding levels of electromagnetic susceptibility (EMS). Similarly, extremely low electromagnetic emission (EME) is achieved by the excellent matching of the output signals.

Key Features

- Fully Compatible with the ISO 11898−2 Standard
- Certified “Authentication on CAN Transceiver Conformance (d1.1)”
- Wide Range of Bus Communication Speed (up to 1 Mbit/s in Function of the Bus 246 T j/F5 1 Tf11lit/s12.ogy.2(0 0 12 59.7543 312.5481 Tm0 Tc286.05 0 1toaeo Tf10 0 0s in)]TJ-.01 Tm0 5]TJ/0 1 Speeds Down to 1 kbit/s

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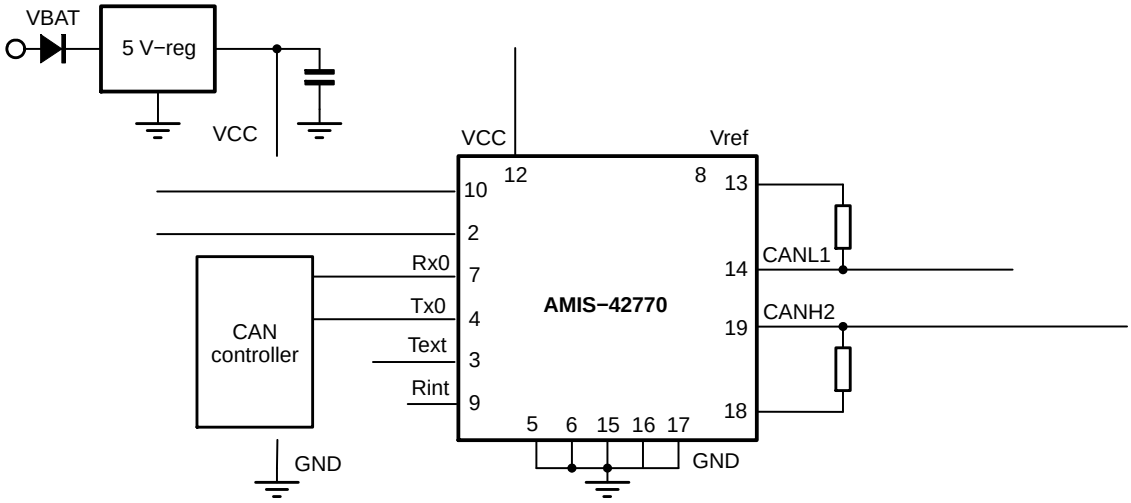

VBAT
5 V−reg
VCC
VCC
Vref
12
8
10
13
2
CANL1
14
Rx0
7
AMIS−42770
Tx0
4
19
CANH2
CAN
controller
Text
3
Rint
9
18
5
6
15
16
17
GND
GND

Table 2. PIN DESCRIPTION

Pin	Name	Description
1	NC	Not connected
2	ENB2	Enable input, bus system 2; internal pull−up
3	Text	Multi−system transmitter Input; internal pull−up
4	Tx0	Transmitter input; internal pull−up
5	GND	Ground connection (Note 2)
6	GND	Ground connection (Note 2)
7	Rx0	Receiver output
8	V_{REF1}	Reference voltage
9	Rint	Multi−system receiver output
10	ENB1	Enable input, bus system 1; internal pull−up
11	NC	Not connected
12	VCC	Positive supply voltage
13	CANH1	CANH transceiver I/O bus system 1
14	CANL1	CANL transceiver I/O bus system 1
15	GND	Ground connection (Note 2)
16	GND	Ground connection (Note 2)
17	GND	Ground connection (Note 2)
18	CANL2	CANL transceiver I/O bus system 2
19	CANH2	CANH transceiver I/O bus system 2
20	NC	Not connected

2. In order to ensure the chip performance, all these pins need to be connected to GND on the PCB.

FUNCTIONAL DESCRIPTION

Overall Functional Description

AMIS−42770 is specially designed to provide the link between the protocol IC (CAN controller) and two physical

Transmitters

The transceiver includes two transmitters, one for each bus line, and a driver control circuit. Each transmitter is implemented as a push and a pull driver. The drivers will be active if the transmission of a dominant bit is required. During the transmission of a recessive bit all drivers are passive. The transmitters have a built−in current limiting circuit that protects the driver stages from damage caused by accidental shor1.8(ces)9.6( )-24 Tc Tc.0078 Tw[(Oo78 Tw[(eiverr78 Tw[(posiccidentcD-.0134 Tn./F3 1 Tf12 0 0 ly1 Tf12 volt To.1962 TD-.0119

Feedback Suppression

The logic unit described in Table 3 constantly ensures that dominant symbols on one bus line are transmitted to the other bus line without imposing any priority on either of the lines. This feature would lead to an “interlock” state with permanent dominant signal transmitted to both bus lines, if no extra measure is taken.

Therefore feedback suppression is included inside the logic unit of the transceiver. This block masks−out reception on that bus line, on which a dominant is actively transmitted. The reception becomes active again only with certain delay after the dominant transmission on this line is finished.

Power−on−Reset (POR)

While Vcc voltage is below the POR level, the POR circuit makes sure that:

- The counters are kept in the reset mode and stable state without current consumption
- Inputs are disabled (don’t care)
- Outputs are high impedant; only Rx0 = high−level
- Analog blocks are in power down
- Oscillator not running and in power down
- CANHx and CANLx are recessive
- VREF output high impedant for POR not released

Over Temperature Detection

A thermal protection circuit is integrated to prevent the transceiver from damage if the junction temperature exceeds thermal shutdown level. Because the transmitters dissipate most of the total power, the transmitters will be switched off only to reduce power dissipation and IC temperature. All other IC functions continue to operate.

Fault Behavior

A fault like a short circuit is limited to that bus line where it occurs; hence data interchange from the protocol IC to the other bus system is not affected.

When the voltage at the bus lines is going out of the normal operating range (−12 V to +12 V), the receiver is not allowed to erroneously detect a dominant state.

Short Circuits

A current−limiting circuit protects the transmitter output stage from damage caused by an accidental short−circuit to either positive or negative supply voltage, although power dissipation increases during this fault condition.

The pins CANHx and CANLx are protected from automotive electrical transients (according to “ISO 7637”).

ELECTRICAL CHARACTERISTICS

Definitions

All voltages are referenced to GND. Positive currents flow into the IC. Sinking current means that the current is flowing into the pin. Sourcing current means that the current is flowing out of the pin.

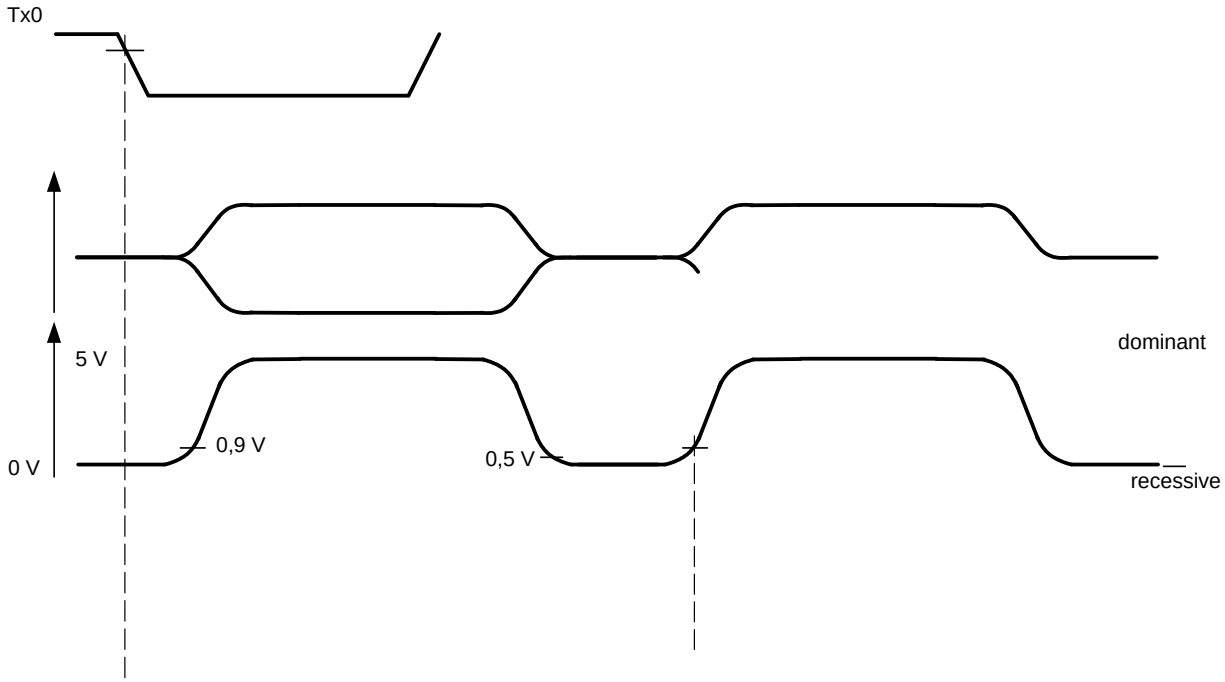
Table 4. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{CC}	Supply voltage		−0.3	+7	V
V_{CANHx}	DC voltage at pin CANH1/2	$0 < V_{CC} < 5.25$ V; no time limit	−45	+45	V
V_{CANLx}	DC voltage at pin CANL1/2	$0 < V_{CC} < 5.25$ V; no time limit	−45	+45	V
V_{digIO}	DC voltage at digital IO pins (EN1B, EN2B, Rint, Rx0, Text, Tx0)		−0.3	V_{CC} + 0.3	V
V_{REF}	DC voltage at pin V_{REF}		−0.3	V_{CC} + 0.3	V
$V_{tran(CANHx)}$	Transient voltage at pin CANH1/2	(Note 4)	−150	+150	V
$V_{tran(CANLx)}$	Transient voltage at pin CANL1/2	(Note 4)	−150	+150	V
$V_{esd(CANLx/CANHx)}$	ESD voltage at CANH1/2 and CANL1/2 pins	(Note 5) (Note 7)	−4 −500	+4 +500	kV V
V_{esd}	ESD voltage at all other pins	(Note 5) (Note 7)	−2 −250	+2 +250	kV V
Latch−up	Static latch−up at all pins	(Note 6)		100	mA
T_{stg}	Storage temperature		−55	+155	°C
T_{amb}	Ambient temperature		−40	+125	°C
T_{junc}					

Table 6. DC AND TIMING CHARACTERISTICS

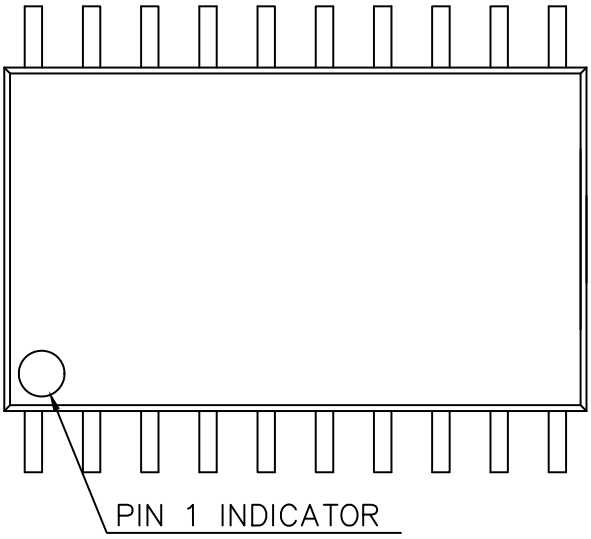
(V_{CC} = 4.75 to 5.25 V; T_{junc} = −40 to +150°C; R_{LT} = 60 W unless specified otherwise.)

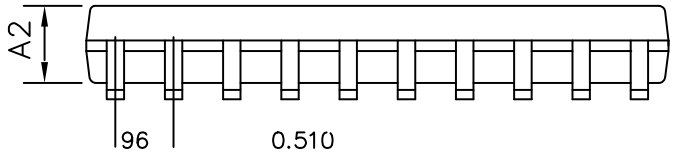
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BUS LINES (pins CANH1/2 and CANL1/2)						
$V_{i(dif)(th)}$	Differential receiver threshold voltage	−5 V < V_{CANLx} < +12 V; −5 V < V_{CANHx} < +12 V; see Figure 7	0.5	0.7	0.9	V
$V_{ihcm(dif)(th)}$	Differential receiver threshold voltage for high common−mode	−35 V < V_{CANLx} < +35 V; −35 V < V_{CANHx} < +35 V; see Figure 7	0.3	0.7	1.05	V
$V_{i(dif)(hys)}$	Differential receiver input voltage hysteresis	−35 V < V_{CANL} < +35 V; −35 V < V_{CANH} < +35 V; see Figure 7	50	70	100	mV
$R_{i(cm)(CANHx)}$	Common−mode input resistance at pin CANH1/2		15	26	37	KΩ
$R_{i(cm)(CANLx)}$	Common−mode input resistance at pin CANL1/2		15	26	37	KΩ
[redacted]	Matching between pin CANH1/2 [redacted] on−	V_{CANHx} = V_{CANLx}	−3	0	+3	%
[redacted]	[redacted] nce		25	50	75	KΩ
[redacted]	CANH1/2	V_{Tx0} = V_{CC}; not tested		7.5	20	pF
$C_{i(CANLx)}$	Input capacitance at pin CANL1/2	V_{Tx0} = V_{CC}; not tested		7.5	20	pF
$C_{i(dif)}$	Differential input capacitance	V_{Tx0} = V_{CC}; not tested		3.75	10	pF
$I_{LI(CANHx)}$	Input leakage current at pin CANH1/2	V_{CC} < PORL_VCC; −5.25 V < V_{CANHx} < 5.25 V	−350	170	350	μA
$I_{LI(CANLx)}$	Input leakage current at pin CANL1/2	V_{CC} < PORL_VCC; −5.25 V < V_{CANLx} < 5.25 V	−350	170	350	μA
$V_{CM−peak}$	Common−mode peak during transition from dom → rec or rec → dom	See Figure 11	−1000		1000	mV
$V_{CM−step}$	Difference in common−mode between dominant and recessive state	See Figure 11	−250		250	mV
THERMAL SHUTDOWN						
$T_{j(sd)}$	Shutdown junction temperature		150			°C
TIMING CHARACTERISTICS (see Figures 8 and 9)						
$t_{d(Tx−BUSon)}$	Delay Tx0/Text to bus active		40	85	120	ns
$t_{d(Tx−BUSoff)}$	Delay Tx0/Text to bus inactive		30	60	115	ns
$t_{d(BUSon−RX)}$	Delay bus active to Rx0/Rint		25	55	115	ns
$t_{d(BUSoff−RX)}$						

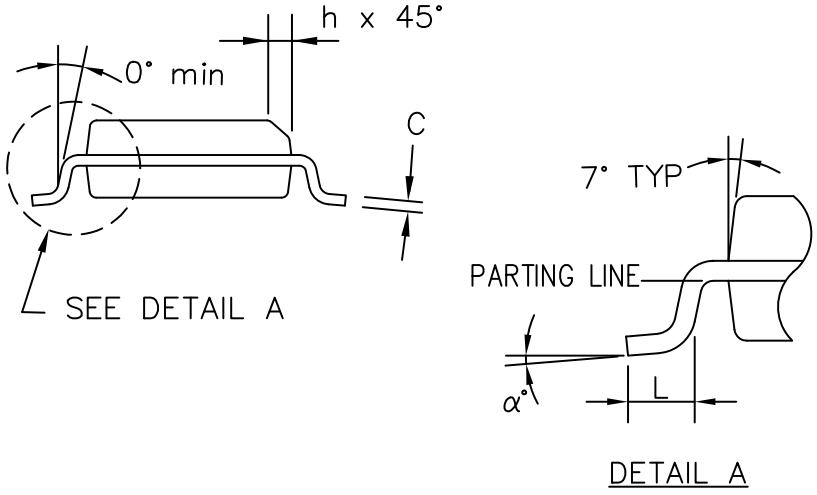

Tx0
5 V
0 V
0,9 V
0,5 V
dominant
recessive

SOIC 20 W
CASE 751AQ 01
ISSUE O

DATE 19 JUN 2008







DETAIL A

DIMENSIONS IN INCHE			
SYMBOL		NOM	MAX.
A	0.093		0.104
A1			0.012
A2	0.088	0.094	0.100
B			
C		00	
D			
E	0.292	0.296	0.299
e		.050 BSC.	
H		0.402	0.419
h	0.010	0.015	0.019
L	0.016	0.033	
	0°	5°	8°