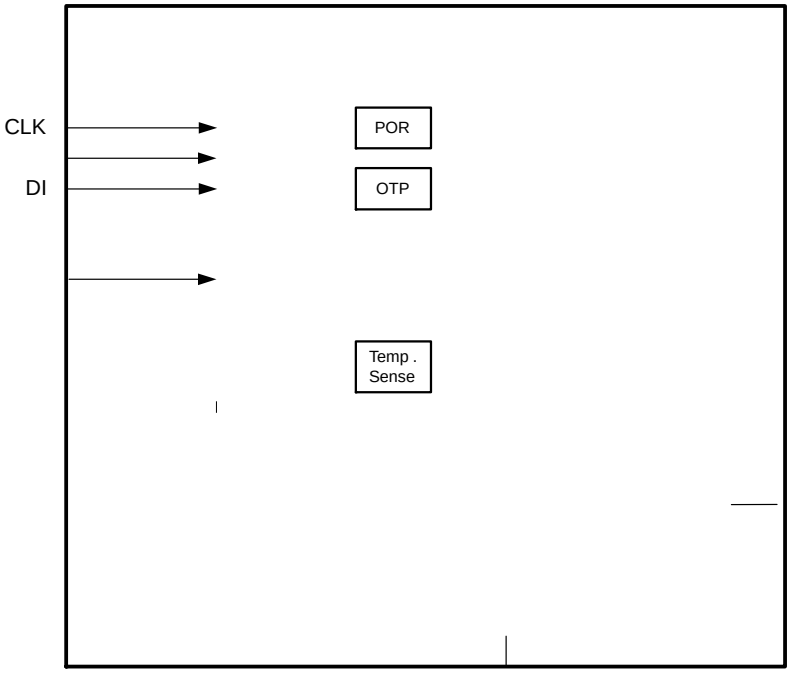
AMIS-30421

Micro-Stepping Stepper Motor Bridge Controller

Introduction

The AMIS−30421 is a micro

BLOCK DIAGRAM



ELECTRICAL SPECIFICATION

Table 2. ABSOLUTE MAXIMUM RATINGS (Notes 1 and 2)

Symbol	Parameter	Min	Max	Unit
V_{BB}	Analog DC supply voltage (Note 3)	−0.3	+40	V
I_{load}	Logic supply external load current, Normal Mode	0	−10	mA
	Logic supply external load current, Sleep Mode	0	−1	mA

Table 4. DC PARAMETERS

The DC parameters are given for V_{BB} and temperature in their operating ranges unless otherwise specified.
Convention: currents flowing in the circuit are defined as positive.

Symbol	Pin(s)	Parameter	Remark/Test Conditions	Min	Typ	Max	Unit
SUPPLY & VOLTAGE REGULATOR							
V_{BB}	VBB	Nominal operating supply range		6		30	V
I_{BB}		Total internal current consumption	Unloaded outputs, I_{INT} included, H−bridge disabled			20	mA
I_{SLEEP}		Sleep mode current consumption	Unloaded outputs, CSb = V_{DD}			150	μA
V_{DD}	VDD						

Table 4. DC PARAMETERS

The DC parameters are given for V_{BB} and temperature in their operating ranges unless otherwise specified.
Convention: currents flowing in the circuit are defined as positive.

Symbol	Pin(s)	Parameter	Remark/Test Conditions	Min	Typ	Max	Unit
PRE DRIVER							
V_{SENS0}	RSENSxx	PWM comparator toggle level 0		78	100	122	mV
V_{SENS1}		PWM comparator toggle level 1		105.3	135	164.7	mV
V_{SENS2}		PWM comparator toggle level 2		156	200	244	mV
V_{SENS3}		PWM comparator toggle level 3		210.6	270	391.4	mV
V_{SENS4}		PWM comparator toggle level 4		261.3	335	408.7	mV
V_{SENS5}		PWM comparator toggle level 5		312	400	488	mV
V_{SENS6}		PWM comparator toggle level 6		390	500	610	mV
V_{SENS7}		PWM comparator toggle level 7		468	600	732	mV
DIGITAL INPUTS							
V_{IL}	CLK, DI, CSb, NXT, DIR, CLR	Logic Low Threshold		0		0.3 x V_{DD}	V
V_{IH}		Logic High Threshold		0.7 x V_{DD}		V_{DD}	V
R_{pd}		Internal Pull Down Resistor	CSb excluded, See also Figure 3	25	50	75	kΩ
R_{pu}	CSb	Internal Pull Up Resistor	See also Figure 3	25	50	75	kΩ
DIGITAL OUTPUTS							
V_{OL}	DO, ERRb, WDb	Logic low output level	Output set to type 4 (see Figure 3)			0.5	V
V_{OH}		Logic high output level		V_{DD} − 0.5			
V_{OL_OPEN}		Logic Low level open drain	I_{OL} = 8 mA, Output set to type 2 (see Figure 3)			0.5	
SPEED AND LOAD ANGLE OUTPUT							
V_{out}							

0.5

Table 4. DC PARAMETERS

The DC parameters are given for V_{BB} and temperature in their operating ranges unless otherwise specified.
Convention: currents flowing in the circuit are defined as positive.

Symbol	Pin(s)	Parameter	Remark/Test Conditions	Min	Typ	Max	Unit
PACKAGE THERMAL RESISTANCE VALUE							
Rth_{ja}		Thermal Resistance Junction−to−Ambient	Simulated Conform JEDEC JESD−51, (2S2P)		30		K/W
			Simulated Conform JEDEC JESD−51, (1S0P)		60		
Rth_{jp}		Thermal Resistance Junction−to−Exposed Pad			0.95		

C PARAMETER The AC parameters are given for V_{BB} and temperature in their operating ranges unless otherwise

Pin(s)	Parameter	Remark/Test Conditions	Min	Typ	Max	Unit
UTS						
	NXT Minimum, high pulse width	See Figure 6	625			ns

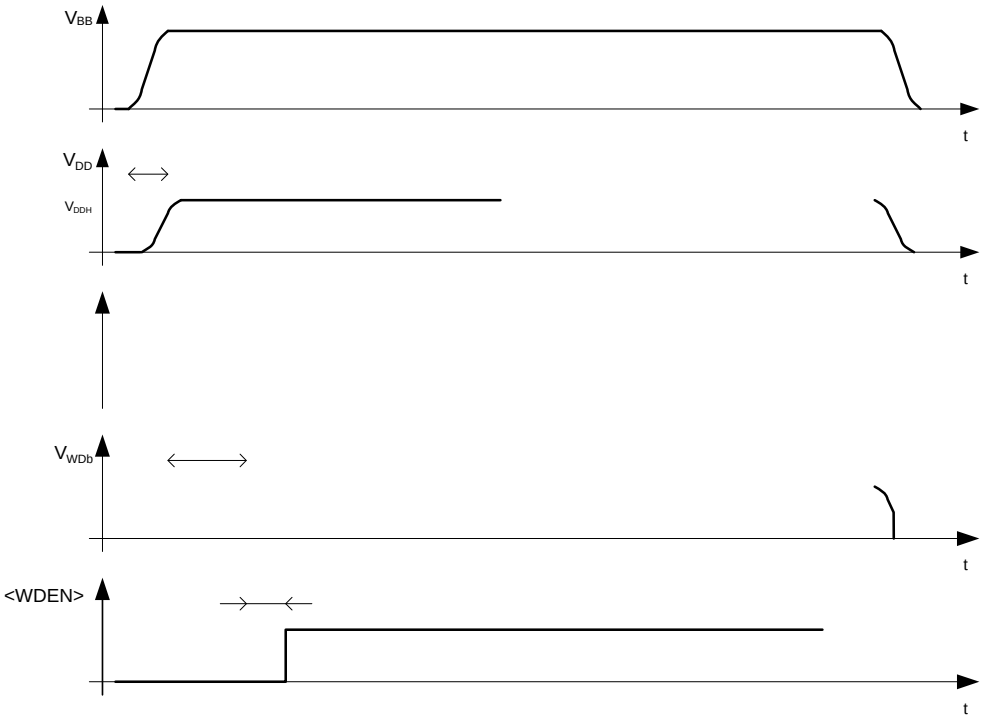

V_{BB}
t
V_{DD}
V_{DDH}
t
V_{WDb}
t
<WDEN>
t

Figure 6. Digital Input Timing Diagram

TYPICAL APPLICATION SCHEMATIC

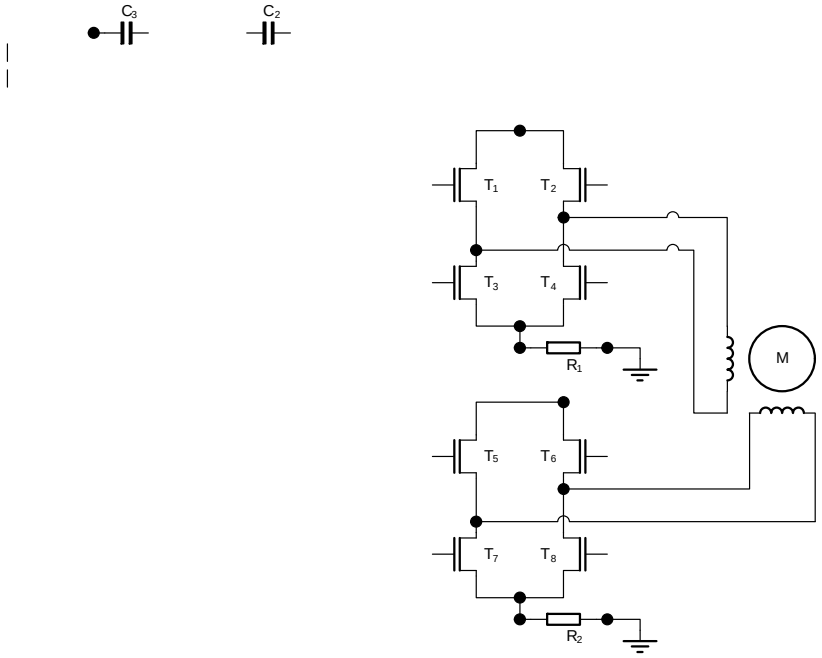


Figure 9. Typical Application Schematic AMIS 30421

FUNCTIONAL DESCRIPTION

H Bridge Pre Drivers

The H−bridge pre−drivers for external N−type MOSFETs

PWM Current Control

A PWM comparator compares continuously the actual winding current (measured over the external sense resistor) with the requested current and feeds back the information to a digital regulation loop. This loop then generates a PWM signal, which turns on/off the current sources (I_{on}, I_{off}) and switches (SW_{on}, SW_{off}). The switching points of the PWM duty−cycle are synchronized to the on−chip PWM clock. The frequency of the PWM controller is fixed and will not vary with changes in the supply voltage. Also variations in motor−speed or load−conditions of the motor have no effect. There are no external components required to adjust the PWM frequency.

For EMC reasons it's possible to add jitter to the PWM by means of the <PWMJ> bit.

Step Translator and Step Mode

The step translator provides the control of the motor by means of the stepmode SPI bits <SM[2:0]>, the enable SPI bit <MOTEN>, the direction SPI bit <DIRCTRL> and input pins DIR and NXT. It is translating consecutive steps in corresponding currents in both motor coils for a given step mode. One out of 8 possible stepping modes can be selected through SPI bits <SM[2:0]>.

After power−up or clear (CLR−pin) the coil current translator is set to position 0. For all stepping modes except full step this means that the coil current is maximum in the Y−coil and zero in the X−coil (see Table 7). If NXT pulses are applied when the DIR−pin is pulled low, SPI bit

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Direction

The direction of rotation can be changed by means of the DIR−pin and the SPI bit <DIRCTRL>. See also Figure 12 up to Figure 15. Setup and hold times need to be respected when changing direction (see Figure 6).

NXT Input

Every rising or falling edge on the NXT−pin (selectable through SPI bit <NXTP>) will move the coil current one step up or down (dependant on the DIR−pin and <DIRCTRL> bit) in the translator table (see Table 7). The motor current will be updated at the next PWM cycle.

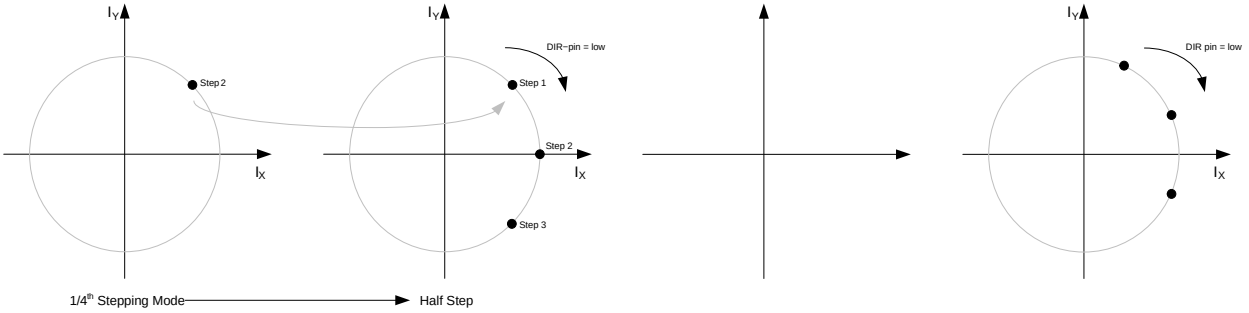
Enable

The enable SPI bit <MOTEN> is used to enable the PWM regulator and drive coil current through the stepper motor coils. When ‘1’ the motor driver is enabled and coil current will be conducted. If ‘0’ (zero), the H−bridge drivers are disabled.

When the motor driver is enabled, the NXT− and DIR−pin as also the <DIRCTRL> SPI bit can be used to control the movement of the stepper motor. It’s not allowed to apply pulses on the NXT−pin when the motor driver is disabled.

Certain errors (see Error Output p24) will automatically disable the motor driver (<MOTEN> = 0). The errors first need to be cleared before one is able to enable the motor driver again.

Setup and hold times need to be respected (see Figure 6).



Correct change to a lower stepping mode. Step 2 of 1/4th stepping mode is equal to Step 1 of half step stepping mode (see Table 7). No offset or phase shift is created.

transient behavior. This transient behavior (which is not the BEMF) can be made visible or invisible on the SLA−pin by means of SPI bit <SLAT>. When set to transparent (<SLAT> = ‘1’), the coil voltage is sampled every PWM cycle and updated on the SLA−pin (see Figure 19). When set to not−transparent (<SLAT> = ‘0’), only the last sample (taken right before leaving the “coil current zero crossing”) will be copied to the SLA−pin (see Figure 20).

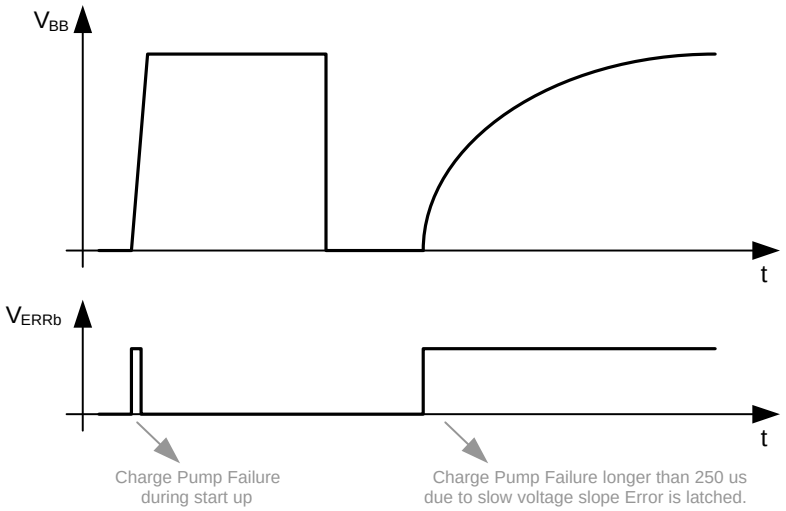


Figure 23. Charge Pump Failure

Watchdog

When V_{BB} is applied, the WDb−pin is kept low for t_{por} (Table 5). This can for instance be used to reset an external microcontroller at power up.

The WDb−pin also has a second function, a Watchdog function. When the watchdog is enabled (<WDEN> = ‘1’), a timer will start counting up. When the counter reaches a certain value (<WDT[3:0]>), the <WD> SPI bit will be set and the WDb−pin will be pulled low for a time equal to t_{POR} to reset the external microcontroller. To avoid that the microcontroller gets reset, the microcontroller needs to re−enable the watchdog before the count value is reached (= write ‘1’ to <WDEN> before <WDT[3:0]> is reached). This functionality can be used to reset a “stuck” microcontroller.

The SPI bit <WD> can be used to detect a cold or warm boot. When powering the application (cold boot), <WD> will be zero. If the microcontroller has been reset by the WDb−pin (warm boot), <WD> bit will be ‘1’. The microcontroller can use this information to detect a cold or warm boot.

It’s forbidden to re−enable the watchdog too fast (minimum time

POWER SUPPLY AND THERMAL CALCULATION

Logic Supply Regulator

AMIS−30421 has an on−chip 3.3V low−drop regulator to supply the digital part of the chip itself, some low−voltage analog blocks and external circuitry. See Table 4 for the limitations.

Over and Undervoltage

AMIS−30421 has undervoltage detection. If V_{BB} drops below V_{BBUL}, the drivers are disabled. To be able to enable the drivers again the V_{BB} voltage needs to rise above V_{BBUH}.

Overvoltage detection is also present. If the voltage rises above V_{BBOH} the drivers are disabled. The voltage needs to drop below V_{BBOL} to be able to enable the driver again. See also Figure 5.

Start Up Behavior

Figure 4 gives the start−up of AMIS−30421. After V_{BB} is applied and after a certain power up time (t_{PU}), the internal voltage regulator V_{DD} will start−up. When V_{DD} gets above V

‘0’. This simple mechanism protects against noise and increases the consistency of the transmitted data. If a parity check error occurs it is recommended to initiate an additional READ command to obtain the status again.

The CSb−pin is active low and may remain low between successive READ commands as illustrated in Figure 28. There is one exception. In case an error condition occurs the root cause of the problem can be determined by reading out the Status Registers. However, if the error occurs at the moment CSb is low, one first needs to pull CSb high to update the Status Registers properly. Only then the Status Registers can be read out to determine the error. For this reason it is also recommended to keep CSb high when the SPI bus is idle.

wants to initiate an SPI transfer to read the Status Registers. Because the internal system clock updates the Status Registers only when CSb line is high, the first read out byte might represent old status information (Figure 30).

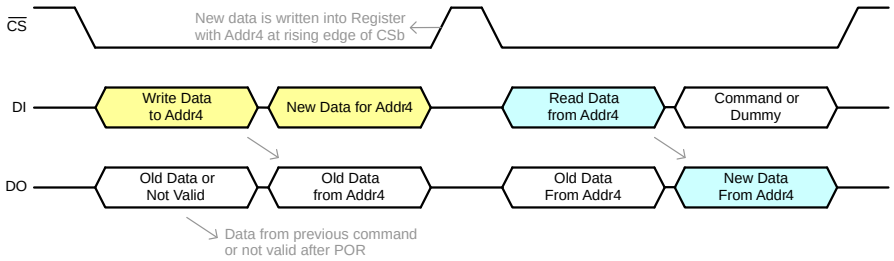


Figure 29. WRITE Operation Followed by a READ operation to verify

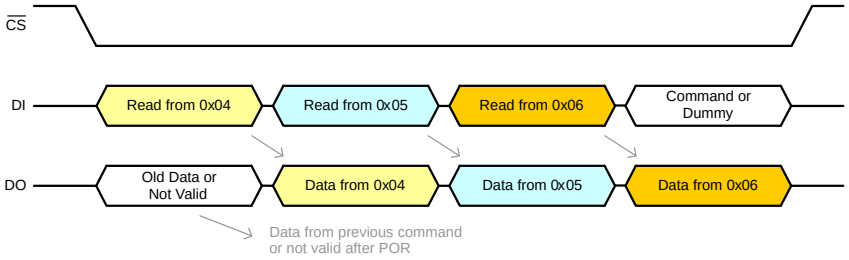


Figure 30. 3 READ Operations in a Row

Bad Examples of READ and WRITE Operations

The following example demonstrates a bad WRITE operation. After a WRITE operation a read operation is done before CSb is made high. The data will not be written in the Register. Figure 32 demonstrates how it should be done (see also Figure 29).

The second example (Figure 33) demonstrates an incorrect way of reading errors. After a WRITE operation the ERRb−pin toggles indication an error. Without toggling CSb the 3 Status Registers are read out to determine the error. Because CSb was not high after the error was detected, the Status Registers will not be updated and the error can not be determined. A second problem with Figure 33 is that the data written to Addr9 will not be stored because CSb was not toggled after the write operation.

Figure 34 gives the correct way of reading out errors. When the error is detected (toggling of ERRb−pin), CSb is made high to make sure the Status Registers are updated. Then the Status Registers are read out. Notice that ERRb toggles after Status Register 1 is read out (Addr 0x05). This indicates that the error was an overcurrent in the X−coil, a charge pump failure or an open X−coil. Also notice that because CSb is made high after the write operation, the write operation will now be done correctly.

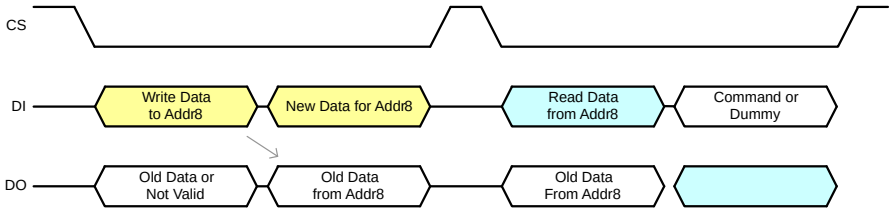

CS
DI
Write Data
to Addr8
New Data for Addr8
Read Data
from Addr8
Command or
Dummy
DO
Old Data or
Not Valid
Old Data
from Addr8
Old Data
From Addr8

Table 8. SPI REGISTER OVERVIEW

SPI Register	Address	Access	Abbreviation
Predriver Register 1	0x0A	R/W	PDRV1
Predriver Register 2	0x0B	R/W	PDRV2
Predriver Register 3	0x0C	R/W	PDRV3
Predriver Register 4	0x0D	R/W	PDRV4
Predriver Register 5	0x0E	R/W	PDRV5
Predriver Register 6	0x0F	R/W	PDRV6
Predriver Register 7	0x10	R/W	PDRV7

Where: R/W = read and write access, R = read access only

Watchdog Register (WR)

The Watchdog Register is located at address 0x00 and can be used to enable the watchdog and set the watchdog time−out. It can also be used to set the short circuit and open coil detection time−out.

Table 9. WATCHDOG REGISTER

Watchdog Register (WR)									
Address		**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
0x00	**Access**	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Reset	0	0	0	0	0	1	0	0
	Data	WDEN	WDT[3:0]				OPEN_COIL[1:0]		−

Table 10. WATCHDOG REGISTER PARAMETERS

Parameter	Value	Value	Description	Info
WDEN	0	Disable	Enables the watchdog	p24
	1	Enable		
WDT[3:0]	0000	32 ms	Defines the watchdog time−out period. The watchdog needs to be re−enabled (WDEN) within this time or WDb−pin is activated for t_{POR}.	p24
	0001	64 ms		
	0010	96 ms		
	0011	128 ms		
	0100	160 ms		
	0101	192 ms		
	0110	224 ms		
	0111	256 ms		
	1000	288 ms		
	1001	320 ms		
	1010	352 ms		
	1011	384 ms		
	1100	416 ms		
	1101	448 ms		
	1110	480 ms		
	1111	512 ms		
OPEN_COIL[1:0]	00	2.56 ms	Defines the open coil detection time−out. If an open coil is detected for a time longer than OpenTimeOut[1:0], an open coil (OPEN_X and/or OPEN_Y) will be reported. Note: Short circuit could trigger open coil detection.	p23
	01	0.32 ms		
	10	20.48 ms		
	11	163.84 ms		

Remark: Bit 0 of Watchdog Register should always be ‘0’ (zero)!

Control Register 0 (CR0)

Control Register 0 is located at address 0x01 and is used to set the maximum coil current and stepping mode. It's also used to set the "coil current zero crossing" duration.

Table 11. CONTROL REGISTER 0

Control Register 0 (CR0)									
Address		**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
0x01	**Access**	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Reset	0	0	0	0	0	0	0	0
	Data	SM[2:0]			MIN_SLA_TIME[1:0]		CUR[2:0]		

Table 12. CONTROL REGISTER 0 PARAMETERS

Parameter	Value	Value	Description	Info
SM[2:0]	000	64th	Defines the 8 stepping modes for the PWM regulator.	p19
	001	32nd		
	010	16th		
	011	8th		
	100	4th		
	101	Half step compensated		
	110	Half step uncompensated		
	111	Full Step		
MIN_SLA_TIME[1:0]	00	40 μs	Defines the minimum "coil current zero crossing" duration. Remark: when NXT frequency gets above PWM frequency (f_{PWM}), MIN_SLA_TIME could be 40us longer.	p20
	01	120 μs		
	10	200 μs		
	11	360 μs		
CUR[2:0]	000	100 mV	Defines the maximum voltage over the coil current sense resistor which defines the maximum coil current. The maximum coil current is calculated as next: I_{coil} = CUR[2:0] / R_{sense}	p20
	001	135 mV		
	010	200 mV		
	011	270 mV		
	100	335 mV		
	101	400 mV		
	110	500 mV		
	111	600 mV		

Control Register 1 (CR1)

Control Register 1 is located at address 0x02 and can used to set the direction, NXT−pin polarity, output configuration of WDb−, ERRb− and DO−pin and to enable PWM jitter. It can also be used to set an additional delay between switching off and on MOSFET's of one half H−bridge (to prevent a short circuit).

Table 13. CONTROL REGISTER 1

Control Register 1 (CR1)									
Address		**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
0x02	**Access**	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Reset	0	0	0	1	0	0	0	1
	Data	DIRCTRL	NXTP	−	IO_OT	−	PWMJ	NO_CROSS[1:0]	

Table 16. CONTROL REGISTER 2 PARAMETERS

Parameter	Value	Value	Description	Info
SLA_OFFS	0	No additional offset	To enable an additional offset on the SLA−pin of 0.6V.	p20
	1	Additional offset of 0.6 V		

Remark: Bit 5 of Control Register 2 should always be ‘0’ (zero)!

Status Register 0 (SR0)

Status Register 0 is located at address 0x04 and can only be read. Status Register 0 is a non−latched register meaning that the value of the register can change without the need of reading out the register. The register can be used to retrieve the temperature range or to verify a watchdog event.
Notice that bit 7 is the parity bit (see READ operation p26).

Table 17. STATUS REGISTER 0

Status Register 0 (SR0)

Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x04	Access	R	R	R	R	R	R	R	R
	Reset	0	0	0	0	0	1	0	0
	Data	PAR	TR[1:0]		WD	−	−	−	−

Table 18. STATUS REGISTER 0 PARAMETERS

Parameter	Value	Value	Description	Info
TR[1:0]	00	−40°C to 15°C	Motor driver thermal range. Remark: TR[1:0] = 11 and TSD = 0 => Thermal Warning TR[1:0] = 11 and TSD = 1 => Thermal Shutdown TSD is located in Status Register 2	p23
	01	15°C to 72°C		
	10	73°C to 150°C		
	11	TSD = 0: 150°C to 170°C TSD = 1: >170°C		
WD	0	No watchdog event	If WDEN = 1 and watchdog not acknowledged before the Watchdog Time−out (WDT[3:0]), WDb−pin will be pulled low for 100ms to reset an external microcontroller and WD bit will be set to ‘1’ to indicate this event. The external microcontroller can use this bit to verify a cold (WD = 0) or warm boot (WD = 1).	p24
	1	Watchdog event occurred		

Status Register 1 (SR1)

Status Register 1 is located at address 0x05 and can only be read. Status Register 1 is a latched register. If an err 1 297.921 .90709 30.61

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Status Register 3 (SR3)

Status Register 3 is located at address 0x07 and can only be read. Status Register 3 contains the microstepping position and can be used to retrieve the position in the translator table (see Table 7). It is a non−latched register meaning that the microstepping position can be updated by the motor driver at any moment. Status Register 3 does not contain a parity bit.

Table 23. STATUS REGISTER 3

Status Register 3 (SR3)									
Address		**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
0x07	**Access**	R	R	R	R	R	R	R	R
	Reset	0	0	0	0	0	0	0	0
	Data	MSP[7:0]							

Table 24. STATUS REGISTER 3 PARAMETERS

Parameter	Value	Value	Description	Info
MSP[7:0]	xxxx xxxx	Microstepping position	Indicates the position within the translator table	p19

Predriver Register 0 (PDRV0)

Predriver Register 0 is located at address 0x09 and can be used to set the current source for the gate charge of the external top MOSFET's during t_1 (see Figure 11).

Table 25. PREDRIVER REGISTER 0

Predriver Register 0 (PDRV0)									
Address		**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
0x09	**Access**	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Reset	0	1	0	1	0	0	1	1
	Data	TOP_ION1[6:3]				−	TOP_ION1[2:0]		

Table 26. PREDRIVER REGISTER 0 PARAMETERS

Parameter	Value	Value	Description	Info
TOP_ION1[6:3]	xxxx	Current source value		

Predriver Register 4 (PDRV4)

Predriver Register 4 is located at address 0x0D and can be used to set the current source for the gate discharge of the external MOSFET's (see Figure 11).

Table 33. PREDRIVER REGISTER 4

Predriver Register 4 (PDRV4)									
Address		**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
0x0D	**Access**	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Reset	0	1	0	0	0	1	0	0
	Data	TOP_IOFF[3:0]				BOT_IOFF[3:0]			

Table 34. PREDRIVER REGISTER 4 PARAMETERS

Parameter	Value	Value	Description	Info
TOP_IOFF[3:0]	xxxx	Current source value	Defines the current source for the external top MOSFET's during t_{off}. Current source can be calculated as next: 10.5 mA + (PDRV4[7:4] x 7 mA)	p13
BOT_IOFF[3 :0]	xxxx	Current source value	Defines the current source for the external bottom MOSFET's during t_{off}. Current source can be calculated as next: 10.5 mA + (PDRV4[3:0] x 7 mA)	p13

Predriver Register 5 (PDRV5)

Predriver Register 5 is located at address 0x0E and can be used to set t_2 (see Figure 11).

Table 35. PREDRIVER REGISTER 5

Predriver Register 5 (PDRV5)									
Address		**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
0x0E	**Access**	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Reset	0	1	0	0	0	1	0	0
	Data	−	TOP_t2[2:0]			−	BOT_t2[2:0]		

Table 36. PREDRIVER REGISTER 5 PARAMETERS

Parameter	Value	Value	Description	Info
TOP_t2[2:0]	000	1.25 μs	Defines the switch on duration t_2 for the external top MOSFET's.	p13
	001	1.75 μs		
	010	2.25 μs		
	011	2.75 μs		
	100	3.25 μs		
	101	3.75 μs		
	110	4.25 μs		
	111111			

Table 36. PREDRIVER REGISTER 5 PARAMETERS

Parameter	Value	Value	Description	Info
BOT_t2[2 :0]	000	1.25 μs	Defines the switch on duration t_2 for the external bottom MOSFET's.	p13
	001	1.75 μs		
	010	2.25 μs		
	011	2.75 μs		
	100	3.25 μs		
	101	3.75 μs		
	110	4.25 μs		
	111	4.75 μs		

Predriver Register 7 (PDRV7)

Predriver Register 7 is located at address 0x10 and can be used to set t_1 (see Figure 11).

Table 39. PREDRIVER REGISTER 7

Predriver Register 7 (PDRV7)									
Address		**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
0x10	**Access**	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Reset	0	0	1	0	0	0	1	0
	Data	−	TOP_t1[2:0]			−	BOT_t1[2:0]		

Table 40. PREDRIVER REGISTER 7 PARAMETERS

Parameter	Value	Value	Description	Info
TOP_t1[2:0]	000	375 ns	Defines the switch on duration t_1 for the external top MOSFET's.	p13
	001	500 ns		
	010	625 ns		
	011	750 ns		
	100	875 ns		

PACKAGE THERMAL CHARACTERISTICS

The AMIS−30421 is available in a NQFP44 package. For cooling optimizations, the NQFP has an exposed thermal pad which has to be soldered to the PCB ground plane. The ground plane needs thermal vias to conduct the heat to the bottom layer.

Figure 35 gives an example of good heat transfer. The exposed thermal pad is soldered directly on the top ground layer (left picture of Figure 35). It's advised to make the top ground layer as large as possible (see arrows Figure 35). To improve the heat transfer even more, the exposed thermal pad is connected to a bottom ground layer by using thermal vias (see right picture of Figure 35). It's advised to make this bottom ground layer as large as possible and with as less as possible interruptions.

For precise thermal cooling calculations the major

443c(.845972287363c6283 w 10 M e3266.96691 g24(i038c352c.011)p98375.2158 re

QFN44 7x7, 0.5P
CASE 485BY
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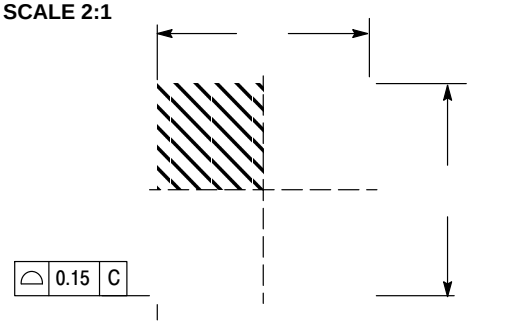
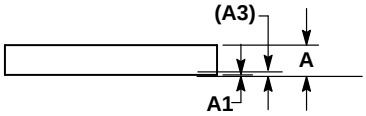
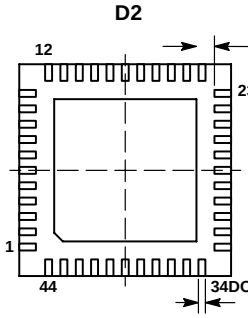
DATE 16 SEP 2011

SCALE 2:1





SEATING
PLANE



34DOCUMENT NUMBER:DESCRIPTION:
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NOTE 3