ADT7483A

Dual Channel Temperature Sensor and Over Temperature Alarm

The ADT7483A is a three-channel digital thermometer and under/over temperature alarm, intended for use in PCs and thermal management systems. It can measure the temperature in two remote locations, for example, the remote thermal diode in a CPU or GPU, or a discrete diode connected transistor. It can also measure its own ambient temperature. The temperature of the remote thermal diode and ambient temperature can be accurately measured to 1 C. The temperature measurement range defaults to 0 C to 127 C, compatible with ADM1032, but can be switched to a wider measurement range, from ĭ64 C to +191 C.

The ADT7483A communicates over a 2-wire serial interface compatible with system management bus (SMBus) standards. The SMBus address is set by the ADD0 and ADD1 pins. As many as nine different SMBus addresses are possible.

An $\overline{\text{ALERT}}$ output signals when the on-chip or remote temperature is outside the programmed limits. The $\overline{\text{THERM}}$ output is a comparator output that allows, for example, on/off control of a cooling fan. The $\overline{\text{ALERT}}$ output can be reconfigured as a second $\overline{\text{THERM}}$ output, if required.

Features

- 1 Local and 2 Remote Temperature Sensors
- 0.25 C Resolution/1 C Accuracy on Remote Channels
- 1 C Resolution/1 C Accuracy on Local Channel
- Extended, Switchable Temperature Measurement Range
  0 C to 127 C (Default) or –64 C to +191 C
- 2-wire SMBus Serial Interface with SMBus Alert Support
- Programmable Over/Under Temperature Limits
- Offset Registers for System Calibration
- Up to 2 Overtemperature Fail-safe $\overline{\text{THERM}}$ Outputs
- Small 16-lead QSOP Package
- 240 μA Operating Current, 5 μA Standby Current
- This Device is Pb-Free, Halogen Free and is RoHS Compliant

Applications

- Desktop and Notebook Computers
- Industrial Controllers
- Smart Batteries
- Automotive
- Embedded Systems
- Burn-in Applications
- Instrumentation

Table 2. ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Unit
	–	
	–	
–	–	
	–	
	–	
–		

Table 5. ELECTRICAL CHARACTERISTICS –

Parameter	Test Conditions	Min	Typ	Max	Unit
Power Supply					
		– –			μ
		–		–	
			–		
Temperature-to-Digital Converter					
	–	– – – –	– – –	–	

TYPICAL PERFORMANCE CHARACTERISTICS

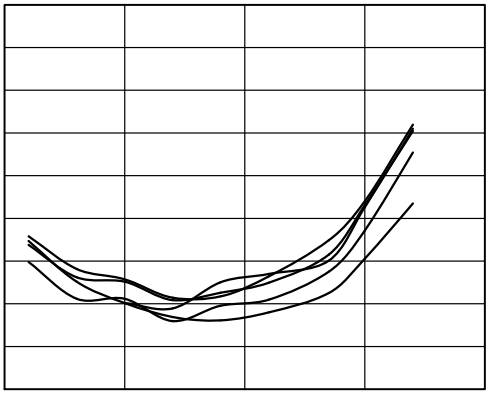


Figure 3. Local Temperature Error vs. Temperature

Figure 4. Remote 1 Temperature Error vs. Temperature

Figure 5. Remote 2 Temperature Error vs. Temperature

Figure 6. Temperature Error vs. D+/D− Leakage Resistance

Figure 7. Temperature Error vs. D+/D− Capacitance

Figure 8. Operating Supply Current vs. Conversion Rate

Theory of Operation

The ADT7483A is a local and 2 remote temperature sensor and over/under temperature alarm. When the ADT7483A is operating normally, the on-board ADC operates in a freerunning mode. The analog input multiplexer alternately selects either the on-chip temperature sensor or one of the remote temperature sensors to measure its local temperature. The ADC digitizes these signals, and the results are stored in the local, Remote 1, and Remote 2 temperature value registers.

The local and remote measurement results are compared with the corresponding high, low, and $\overline{\text{THERM}}$ temperature limits stored in on-chip registers. Out-of-limit comparisons generate flags that are stored in the status register. A result that exceeds the high temperature limit, the low temperature limit, or a remote diode open circuit causes the $\overline{\text{ALERT}}$ output to assert low. Likewise, exceeding $\overline{\text{THERM}}$

Table 6. REGISTER ADDRESS FOR THE TEMPERATURE VALUES

Temperature Channel	Register Address, MSBs	Register Address, LSBs

By setting Bit 3 of the Configuration 1 Register to 1, the Remote 2 temperature values can be read from the following register addresses:

Remote 2, MSBs = 0x01
Remote 2, LSBs = 0x10

The above is true only when Bit 3 of the Configuration 1 register is set. To read the Remote 1 temperatures, this bit needs to be switched back to 0.

Only the two MSBs in the remote temperature low byte are used. This gives the remote temperature measurement a resolution of 0.25 C. Table 7 shows the data format for the remote temperature low byte.

Table 7. EXTENDED TEMPERATURE RESOLUTION (REMOTE TEMPERATURE LOW BYTE)

Extended Resolution	Remote Temperature Low Byte

When reading the full remote temperature value, both the high and low byte, the two registers should be read LSB first and then the MSB. This is because reading the LSB will cause the MSB to be locked until it is read, guaranteeing that the two values read are a result of the same temperature measurement.

Temperature Measurement Range

The temperature measurement range for both local and remote measurements is, by default, 0 C to 127 C. However, the ADT7483A can be operated using an extended temperature range from ĭ64 C to +191 C. This means, the ADT7483A can measure the full temperature range of a remote thermal diode, from ĭ55 C to +150 C. The user can switch between these two temperature ranges by setting or clearing Bit 2 in the Configuration 1 register. A valid result is available in the next measurement cycle after changing the temperature range.

In extended temperature mode, the upper and lower temperatures that can be measured by the ADT7483A are limited by the remote diode selection. The temperature registers themselves can have values from ĭ64 C to +191 C. However, most temperature sensing diodes have a maximum temperature range of ĭ55 C to +150 C.

Note that althouT815.9307 440.8441 Tm-.0007 Tce full temperature

Registers

The registers in the ADT7483A are eight bits wide. These registers are used to store the results of remote and local temperature measurements, and high and low temperature limits, and to configure and control the device. A description of these registers is provided in this section.

Address Pointer Register

The address pointer register does not have, nor does it require, an address because the first byte of every write operation is automatically written to this register. The data in this first byte always contains the address of another register on the ADT7483A, which is stored in the address pointer register. It is to this other register address that the second byte of a write operation is written, or to which a subsequent read operation is performed.

The power-on default value of the address pointer register is 0x00, so if a read operation is performed immediately after

Conversion Rate/Channel Selector Register

The conversion rate/channel selector register is at Address 0x04 for reads, and Address 0x0A for writes. The four LSBs of this register are used to program the conversion times from 15.5 ms (Code 0x0A) to 16 seconds (Code 0x00). To program the ADT7483A to perform

Table 12. STATUS REGISTER 1 BIT ASSIGNMENTS

Bit	Mnemonic	Function	$\overline{\text{ALERT}}$

Table 13. STATUS REGISTER 2 BIT ASSIGNMENTS

Bit	Mnemonic	Function	$\overline{\text{ALERT}}$

The eight flags that can generate an $\overline{\text{ALERT}}$ are NOR'd together, so if any of them are high, the $\overline{\text{ALERT}}$ interrupt latch is set and the $\overline{\text{ALERT}}$ output goes low (provided they are not masked out).

Reading the Status 1 register will clear the five flags, Bit 6 to Bit 2 in Status Register 1, provided the error conditions that caused the flags to be set have gone away. Reading the Status 2 register will clear the three flags, Bit 4 to Bit 2 in Status Register 2, provided the error conditions that caused the flags to be set have gone away. A flag bit can only be reset if the corresponding value register contains an in-limit measurement or if the sensor is good.

The $\overline{\text{ALERT}}$ interrupt latch is not reset by reading the status register. It is reset when the $\overline{\text{ALERT}}$ output has been serviced by the master reading the device address, provided the error condition has gone away and the status register flag bits have been reset.

When Flag 1 and/or Flag 0 of Status Register 1, or Flag 1 of Status Register 2 are set, the $\overline{\text{THERM}}$ output goes low to indicate that the temperature measurements are outside the programmed limits. The $\overline{\text{THERM}}$ output does not need to be reset, unlike the $\overline{\text{ALERT}}$ output. Once the measurements are within the limits, the corresponding status register bits are automatically reset and the $\overline{\text{THERM}}$ output goes high. The user may add hysteresis by programming Register 0x21. The $\overline{\text{THERM}}$ output will be reset only when the temperature falls below the $\overline{\text{THERM}}$ limit minus hysteresis.

When Pin 13 is configured as $\overline{\text{THERM2}}$, only the high temperature limits are relevant. If Flag 6, Flag 4 of Status Register 1, or Flag 4 of Status Register 2 are set, the $\overline{\text{THERM2}}$ output goes low to indicate that the temperature measurements are outside the programmed limits. Flag 5 and Flag 3 of Status Register 1, and Flag 3 of Status Register 2 have no effect on $\overline{\text{THERM2}}$. The behavior of $\overline{\text{THERM2}}$ is otherwise the same as $\overline{\text{THERM}}$.

Bit 0 of Status Register 2 is set whenever the $\overline{\text{ALERT}}$ output of the ADT7483A is asserted low. This means that the user need only read Status Register 2 to determine if the ADT7483A is responsible for the $\overline{\text{ALERT}}$. Bit 0 of Status Register 2 is reset when the $\overline{\text{ALERT}}$ output is reset. If the $\overline{\text{ALERT}}$ output is masked, then this bit is not set.

Offset Register

Offset errors may be introduced into the remote temperature measurement by clock noise or by the thermal diode being located away from the hot spot. To achieve the specified accuracy on this channel, these offsets must be removed.

The offset values are stored as 10-bit, twos complement values:

The Remote 1 offset MSBs are stored in Register 0x11, and the LSBs are stored 0x12 (low byte, left justified).

The Remote 2 offset MSBs are stored in Register 0x34, and the LSBs are stored 0x35 (low byte, left justified).

The Remote 2 offset can be written to, or read from, the Remote 1 offset registers if Bit 3 of the Configuration 1 register is set to 1. This bit should be set to 0 (default) to read the Remote 1 offset values.

Only the upper 2 bits of the LSB registers are used. The MSB of the MSB offset registers is the sign bit. The minimum offset that can be programmed is ĭ128 C, and the maximum is +127.75 C.

The value in the offset register is added or subtracted to the measured value of the remote temperature.

The offset register powers up with a default value of 0 C and will have no effect unless the user writes a different value to it.

ADT7483A

The serial bus protocol operates as follows:

1. The master initiates data transfer by establishing a start condition, defined as a high-to-low transition on the serial data line (SDATA), while the serial clock line (SCLK) remains high. This indicates that an address/data stream follows. All slave peripherals connected to the serial bus respond to the start condition and shift in the next eight bits, consisting of a 7-bit address (MSB first) plus an R/$\overline{W}$ bit, which determines the direction of the data transfer, that is, whether data will be written to, or read from, the slave device. The peripheral whose address corresponds to the transmitted address responds by pulling the data line low during the low period before the ninth clock pulse, known as the acknowledge bit. All other devices on the bus now remain idle while the selected device waits for data to be read from or written to it. If the R/$\overline{W}$ bit is a 0, the master writes to the slave device. If the R/$\overline{W}$ bit is a 1, the master reads from the slave device.
2. Data is sent over the serial bus in a sequence of nine clock pulses, eight bits of data followed by an acknowledge bit from the slave device. Transitions on the data line must occur during the low period of the clock signal and remain stable during the high period, since a low-to-high transition when the clock is high may be interpreted as a stop signal. The number of data bytes that can be transmitted over the serial bus in a single read or write operation is limited only by what the master and slave devices can handle.
3. When all data bytes have been read or written, stop conditions are established. In write mode, the master will pull the data line high during the tenth clock pulse to assert a stop condition. In read mode, the master device will override the acknowledge bit by pulling the data line high during the low period before the ninth clock pulse. This is known as no acknowledge. The master will then take the data line low during the low period before the tenth clock pulse, then high during the tenth clock pulse to assert a stop condition.

Any number of bytes of data may be transferred over the serial bus in one operation, but it is not possible to mix read and write in one operation because the type of operation is determined at the beginning and cannot subsequently be changed without starting a new operation. For the ADT7483A, write operations contain either one or two bytes, while read operations contain one byte.

To write data to one of the device data registers, or to read data from it, the address pointer register must be set so that the correct data register is addressed. The first byte of a write operation always contains a valid address that is stored in the address pointer register. If data is to be written to the device, the write operation contains a second data byte that is written to the register selected by the address pointer register (see Figure 15).

The device address is sent over the bus followed by R/$\overline{W}$ set to 0. This is followed by two data bytes. The first data byte is the address of the internal data register to be written to, which is stored in the address pointer register. The second data byte is the data to be written to the internal data register.

Figure 15. Writing a Register Address to the Address Pointer Register, then Writing Data to the Selected Register

remains low, the master will send the ARA again, and so on, until all devices whose $\overline{\text{ALERT}}$ outputs were low have responded.

Masking the $\overline{\text{ALERT}}$ Output

The $\overline{\text{ALERT}}$ output can be masked for local, Remote 1, Remote 2, or all three channels. This is done by setting the appropriate mask bits in either the Configuration 1 register (read address = 0x03, write address = 0x09) or in the consecutive $\overline{\text{ALERT}}$ register (address = 0x22)

To mask $\overline{\text{ALERT}}$s due to local temperature, set Bit 5 of the consecutive $\overline{\text{ALERT}}$ register to 1. Default = 0.

To mask $\overline{\text{ALERT}}$s due to Remote 1 temperature, set Bit 1 of the Configuration 1 register to 1. Default = 0.

To mask $\overline{\text{ALERT}}$s due to Remote 2 temperature, set Bit 0 of the Configuration 1 register to 1. Default = 0.

To mask $\overline{\text{ALERT}}$s due to any channel, set Bit 7 of the Configuration 1 register to 1. Default = 0.

Low Power Standby Mode

The ADT7483A can be put into low power standby mode by setting Bit 6 (Mon/STBY bit) of the Configuration 1 register (read address = 0x03, write address = 0x09) to 1. When Bit 6 is 0, the ADT7483A operates normally. When Bit 6 is 1, the ADC is inhibited, and any conversion in progress is terminated without writing the result to the corresponding value register.

The SMBus is still enabled. Power consumption in the standby mode is reduced to less than 5 μA.

When the device is in standby mode, it is still possible to initiate a one-shot conversion of both channels by writing to the oneshot register (Address 0x0F), after which the device will return to standby. It does not matter what is written to the one-shot register, all data written to it is ignored.

It is also possible to write new values to the limit register while in standby mode. If the values stored in the temperature value registers are now outside the new limits, an $\overline{\text{ALERT}}$ is generated, even though the ADT7483A is still in standby.

Sensor Fault Detection

The ADT7483A has internal sensor fault detection circuitry located at its D+ input. This circuit can detect situations where a remote diode is not connected, or is incorrectly connected, to the ADT7483A. A simple voltage comparator trips if the voltage at D+ exceeds V_{DD} ǐ 1 V (typical), signifying an open circuit between D+ and Dǐ. The output of this comparator is checked when a conversion is initiated. Bit 2 (D1 OPEN flag) of the Status Register 1 (Address 0x02) is set if a fault is detected on the Remote 1 channel. Bit 2 (D2 OPEN flag) of the Status Register 2 (Address 0x23) is set if a fault is detected on the Remote 2 channel. If the $\overline{\text{ALERT}}$ pin is enabled, setting this flag will cause $\overline{\text{ALERT}}$ to assert low.

If a remote sensor is not used with the ADT7483A, then the D+ and Dǐ inputs of the ADT7483A need to be tied together to prevent the OPEN flag from being continuously set.

Most temperature sensing diodes have an operating temperature range of ǐ55 C to +150 C. Above 150 C, they lose their semiconductor characteristics and approximate conductors instead. This results in a diode short, setting the OPEN flag. The remote diode in this case no longer gives an accurate temperature measurement. A read of the temperature result register will give the last good temperature measurement. The user should be aware that, while the diode fault is triggered, the temperature measurement on the remote channels may not be accurate.

Interrupt System

The ADT7483A has two interrupt outputs, $\overline{\text{ALERT}}$ and $\overline{\text{THERM}}$. Both outputs have different functions and behavior. $\overline{\text{ALERT}}$ is maskable and responds to violations of software programmed temperature limits or an open-circuit fault on the remote diode. $\overline{\text{THERM}}$ is intended as a fail-safe interrupt output that cannot be masked.

If the Remote 1, Remote 2, or local temperature exceeds the programmed high temperature limits, or equals or exceeds the low temperature limits, the $\overline{\text{ALERT}}$ output is asserted low. An open-circuit fault on the remote diode also causes $\overline{\text{ALERT}}$ to assert. $\overline{\text{ALERT}}$ is reset when serviced by a master reading its device address, provided the error condition has gone away and the status register has been reset.

Similarly, the $\overline{\text{THERM}}$ output asserts low if the Remote 1, Remote 2, or local temperature exceeds the programmed $\overline{\text{THERM}}$ limits. The $\overline{\text{THERM}}$ temperature limits should normally be equal to or greater than the high temperature limits. $\overline{\text{THERM}}$ is automatically reset when the temperature falls back within the ($\overline{\text{THERM}}$ ǐ Hysteresis) limit. The local and remote $\overline{\text{THERM}}$ limits are set by default to 85 C. An hysteresis value can be programmed, in which case, $\overline{\text{THERM}}$ resets when the temperature falls to the limit value minus the hysteresis value. This applies to both local and remote measurement channels. The power-on hysteresis default value is 10 C, but this may be reprogrammed to any value after power-up.

The hysteresis loop on the $\overline{\text{THERM}}$ outputs is useful when $\overline{\text{THERM}}$ is used for on/off control of a fan. The user's system can be set up so that when $\overline{\text{THERM}}$ asserts, a fan can be switched on to cool the system. When $\overline{\text{THERM}}$ goes high again, the fan can be switched off. Programming an hysteresis value protects from fan jitter, wherein the temperature hovers around the $\overline{\text{THERM}}$ limit and the fan is constantly being switched.

Table 18. $\overline{\text{THERM}}$ HYSTERESIS

$\overline{\text{THERM}}$ Hysteresis	Binary Representation

Figure 19 shows how the $\overline{\text{THERM}}$ and $\overline{\text{ALERT}}$ outputs operate. The $\overline{\text{ALERT}}$ output can be used as an $\overline{\text{SMBALERT}}$

Applications

Noise Filtering

For temperature sensors operating in noisy environments, previous practice was to place a capacitor across the D+ and Dĭ pins to help combat the effects of noise. However, large capacitances affect the accuracy of the temperature measurement, leading to a recommended maximum capacitor value of 1,000 pF.

Factors Affecting Diode Accuracy

Remote Sensing Diode

The ADT7483A is designed to work with substrate transistors built into processors or with discrete transistors. Substrate transistors will generally be PNP types with the collector connected to the substrate. Discrete types can be either a PNP or NPN transistor connected as a diode (base shorted to collector). If an NPN transistor is used, the collector and base are connected to D+ and the emitter to Dĭ. If a PNP transistor is used, the collector and base are connected to Dĭ and the emitter to D+.

To reduce the error due to variations in both substrate and discrete transistors, the following factors should be taken into consideration:

The ideality factor, n_f, of the transistor is a measure of the deviation of the thermal diode from ideal behavior. The ADT7483A is trimmed for an n_f value of 1.008. Use the following equation to calculate the error introduced at a temperature,T (C) when using a transistor whose n_f does not equal 1.008. Consult the processor data sheet for the n_f values.

$$\Delta = \left(- \right) / \times \left(+ \right)$$

To factor this in, write the DT value to the offset register. It is then automatically added to, or subtracted from, the temperature measurement by the ADT7483A.

Figure 21. Typical Arrangement of Signal Tracks

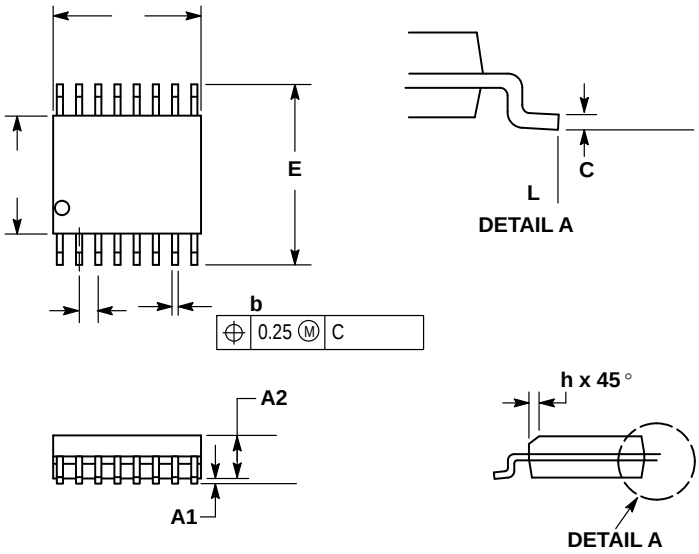
3. Minimize the number of copper/solder joints that can cause thermocouple effects. Where copper/solder joints are used, make sure that they are in both the D+ and Dĭ path and at the same temperature.
   Thermocouple effects should not be a major problem as 1 C corresponds to approximately 200 mV, and thermocouple voltages are about 3 mV/ C of temperature difference. Unless there are two thermocouples with a large temperature differential between them, thermocouple voltages should be much less than 200 mV.
4. Place a 0.1 μF bypass capacitor close to the V_{DD} pin. In extremely noisy environments, place an input filter capacitor across D+ and Dĭ close to the ADT7483A. This capacitance can effect the temperature measurement, so care must be taken to ensure that any capacitance seen at D+ and Dĭ is a maximum of 1,000 pF. This maximum value includes the filter capacitance, plus any cable or stray capacitance between the pins and the sensor diode.
5. If the distance to the remote sensor is more than 8 inches, the use of twisted pair cable is recommended. A total of 6 feet to 12 feet is needed.
6. For very long distances (up to 100 feet), use shielded twisted pair, such as Belden No. 8451 microphone cable. Connect the twisted pair to D+ and Dĭ, and the shield to GND close to the ADT7483A. Leave the remote end of the shield unconnected to avoid ground loops.

Because the measurement technique uses switched current sources, excessive cable or filter capacitance can affect the measurement. When using long cables, the filter capacitance can be reduced or removed.

QSOP16
CASE 492−01
ISSUE A

DATE 23 MAR 2011

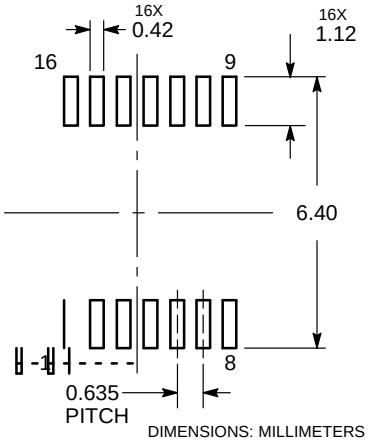
SCALE 2:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.005 PER SIDE. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.005 PER SIDE. D AND E1 ARE DETERMINED AT DATUM H.
5. DATUMS A AND B ARE DETERMINED AT DATUM H.

	INCHES	
DIM	**MIN**	**MAX**
A	0.053	0.069
A1	0.004	0.010
b	0.008	0.012
c	0.007	0.010
e	0.025 BSC	
h	0.009	0.020
L	0.016	0.050
M	0°	8°

SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

XXXXX = Specific Device Code
YY = Year
WW = Work Week
G = Pb−Free Package