ADP3120A

Dual Bootstrapped, 12 V MOSFET Driver with Output Disable

The ADP3120A is a single Phase 12 V MOSFET gate drivers optimized to drive the gates of both high−side and low−side power MOSFETs in a synchronous buck converter. The high−side and low−side driver is capable of driving a 3000 pF load with a 45 ns propagation delay and a 25 ns transition time.

With a wide operating voltage range, high or low side MOSFET gate drive voltage can be optimized for the best efficiency. Internal adaptive nonoverlap circuitry further reduces switching losses by preventing simultaneous conduction of both MOSFETs.

The floating top driver design can accommodate VBST voltages as high as 35 V, with transient voltages as high as 40 V. Both gate outputs can be driven low by applying a low logic level to the Output Disable ($\overline{OD}$) pin. An Undervoltage Lockout function ensures that both driver outputs are low when the supply voltage is low, and a Thermal Shutdown function provides the IC with overtemperature protection.

Features

- All−In−One Synchronous Buck Driver
- Bootstrapped High−Side Drive
- One PWM Signal Generates Both Drives
- Anticross Conduction Protection Circuitry
- $\overline{OD}$ for Disabling the Driver Outputs Meets CPU VR Requirement when Used with Patented FlexMode™ Controller
- These are Pb−Free Devices

Applications

- Multiphase Desktop CPU Supplies
- Single−Supply Synchronous Buck Converters

MARKING DIAGRAMS

A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

August, 2018 − Rev. 5
Publication Order Number:
ADP3120A/D

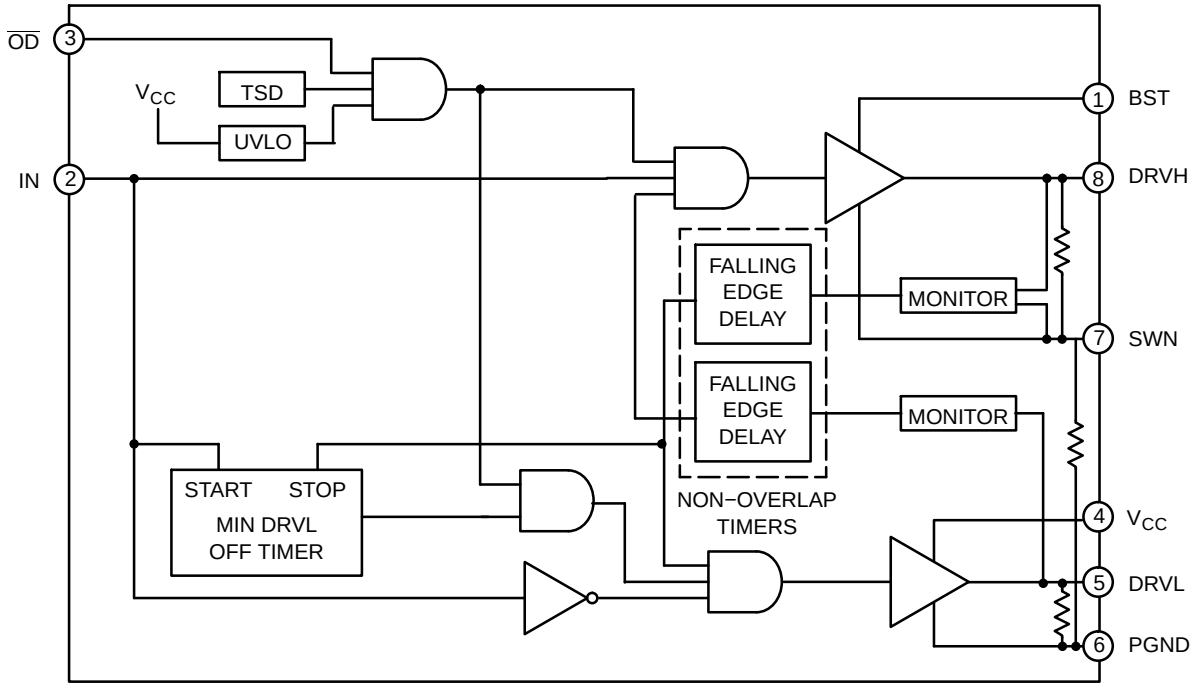


Figure 1. Block Diagram

PIN DESCRIPTION

SO−8	DFN8	Symbol	Description
1	1	BST	Upper MOSFET Floating Bootstrap Supply. A capacitor connected between BST and SW pins holds this bootstrap voltage for the high−side MOSFET as it is switched. The recommended capacitor value is between 100 nF and 1.0 μF. An external diode is required with the ADP3120A.
2	2	IN	Logic−Level Input. This pin has primary control of the drive outputs.
3	3	$\overline{OD}$	Output Disable. When low, normal operation is disabled forcing DRVH and DRVL low.
4	4	V_{CC}	Input Supply. A 1.0 μF ceramic capacitor should be connected from this pin to PGND.
5	5	DRVL	Output drive for the lower MOSFET.
6	6	PGND	Power Ground. Should be closely connected to the source of the lower MOSFET.
7	7	SWN	Switch Node. Connect to the source of the upper MOSFET.
8	8	DRVH	Output drive for the upper MOSFET.

MAXIMUM RATINGS

Rating		Value	Unit
Operating Ambient Temperature, T_A		−20 to 85	°C
Operating Junction Temperature, T_J (Note 1)		−20 to 150	°C
Package Thermal Resistance: SO−8 Junction−to−Case, $R_{\theta JC}$ Junction−to−Ambient, $R_{\theta JA}$ (2−Layer Board) Package Thermal Resistance: DFN8 (Note 2) Junction−to−Case, $R_{\theta JC}$ (From die to exposed pad) Junction−to−Ambient, $R_{\theta JA}$		 45 123 7.5 55	 °C/W °C/W °C/W °C/W
Storage Temperature Range, T_S		−65 to 150	°C
Lead Temperature Soldering (10 sec): Reflow (SMD styles only)	Pb−Free (Note 3)	260 peak	°C
JEDEC Moisture Sensitivity Level	SO−8 (260 peak profile)	1	−

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Internally limited by thermal shutdown, 150°C min.
2. 2 layer board, 1 in^2 Cu, 1 oz thickness.
3. 60−180 seconds minimum above 237°C.

NOTE: This device is ESD sensitive. Use standard ESD precautions when handling.

MAXIMUM RATINGS

Pin Symbol	Pin Name	V_{MAX}	V_{MIN}
V_{CC}	Main Supply Voltage Input	15 V	−0.3 V
PGND	Ground	0 V	0 V
BST	Bootstrap Supply Voltage Input	35 V wrt/PGND 40 V < 50 ns wrt/PGNDC.	

ELECTRICAL CHARACTERISTICS (Note 4) (V_{CC} = 12 V, T_A = −20°

APPLICATIONS INFORMATION

Theory of Operation

The ADP3120A are single phase MOSFET drivers designed for driving two N−channel MOSFETs in a synchronous buck converter topology. The ADP3120A will operate from 5.0 V or 12 V, but have been optimized for high current multi−phase buck regulators that convert 12 V rail directly to the core voltage required by complex logic chips. A single PWM input signal is all that is required to properly drive the high−side and the low−side MOSFETs. Each driver is capable of driving a 3 nF load at frequencies up to 1 MHz.

Low−Side Driver

The low−side driver is designed to drive a ground−referenced low $R_{DS(on)}$ N−Channel MOSFET. The voltage rail for the low−side driver is internally connected to the V_{CC} supply and PGND.

High−Side Driver

The high−side driver is designed to drive a floating low $R_{DS(on)}$ N−channel MOSFET. The gate voltage for the high side driver is developed by a bootstrap circuit referenced to Switch Node (SW) pin.

The bootstrap circuit is comprised of an external diode, and an external bootstrap capacitor. When the ADP3120A are starting up, the SW pin is at ground, so the bootstrap capacitor will charge up to V_{CC} through the bootstrap diode See Figure 4. When the PWM input goes high, the high−side driver will begin to turn on the high−side MOSFET using the stored charge of the bootstrap capacitor. As the high−side MOSFET turns on, the SW pin will rise. When the high−side MOSFET is fully on, the switch node will be at 12 V, and the BST pin will be at 12 V plus the charge of the bootstrap capacitor (approaching 24 V).

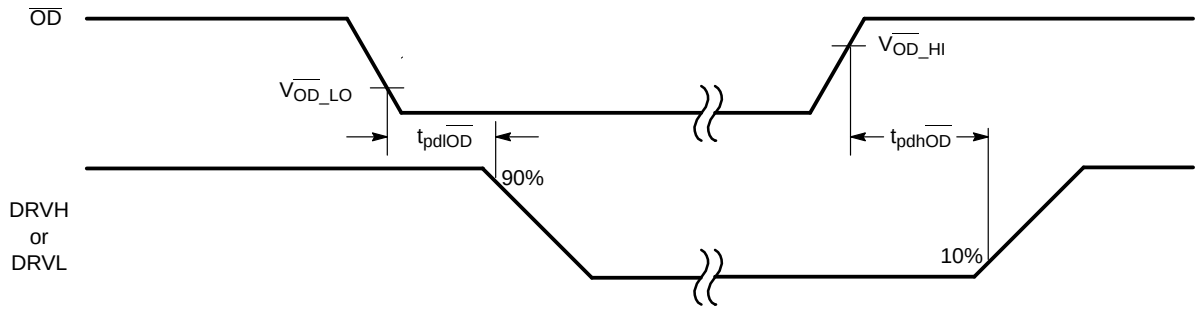


Figure 2. Output Disable Timing Diagram

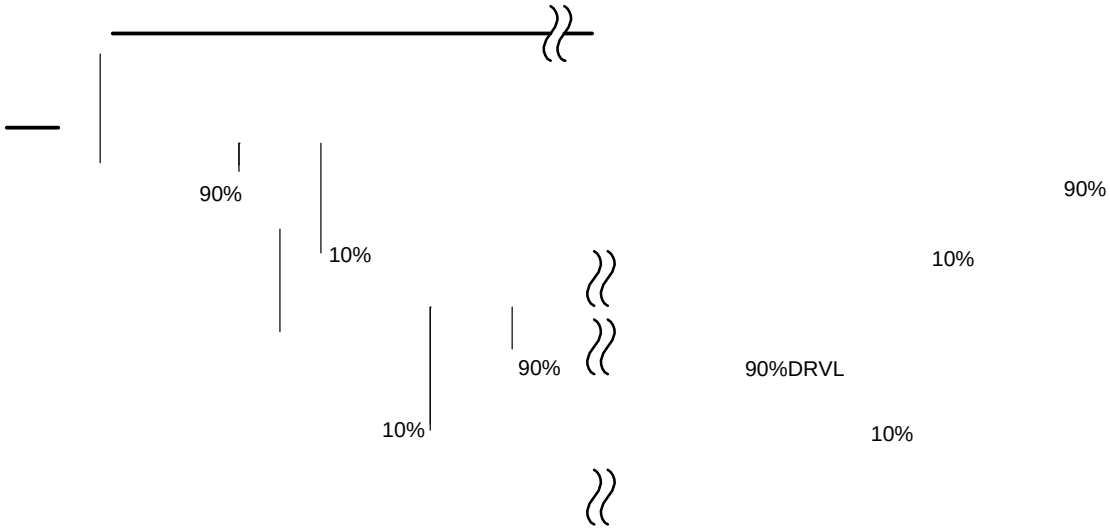
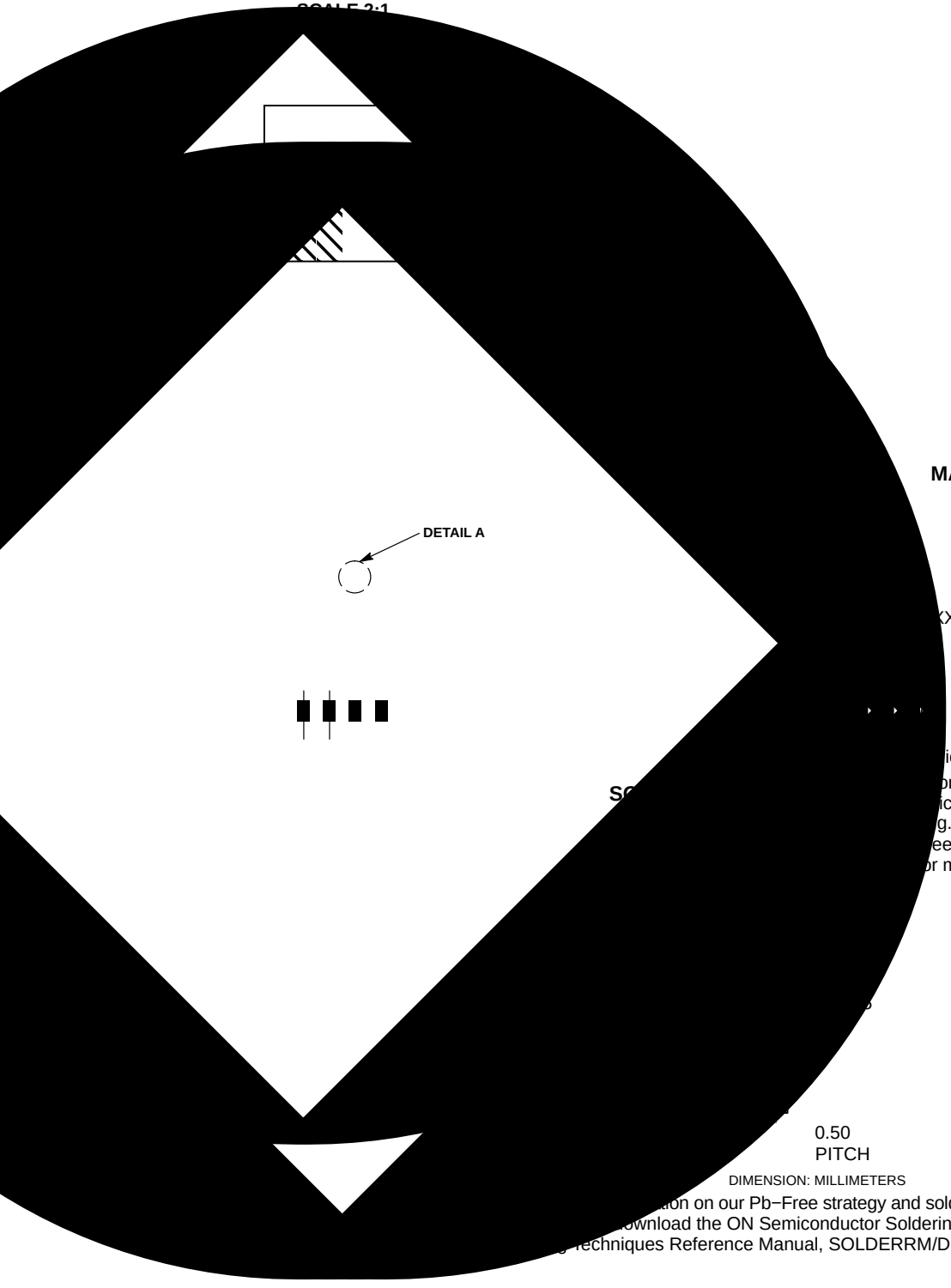


Figure 3. Nonoverlap Timing Diagram

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

DFN8 3x3, 0.5P
CASE 506BJ−01
ISSUE O

DATE 08 NOV 2007



GENERIC
MARKING DIAGRAM*

8

XXX = Specific Device Code
= Assembly Location
= Wafer Lot
= Year
= Work Week
= Pb−Free Package

icrodot may be in either location)

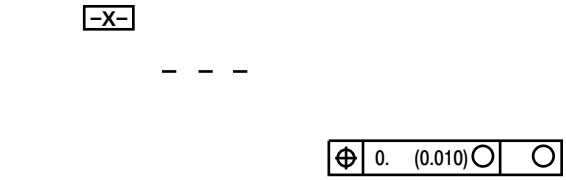
ormation is generic. Please refer
ice data sheet for actual part
g.

ee indicator, “G” or microdot “ ▪”,
r may not be present.

0.50
PITCH

DIMENSION: MILLIMETERS

tion on our Pb−Free strategy and soldering
ownload the ON Semiconductor Soldering and
Techniques Reference Manual, SOLDERRM/D.



C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0	8	0	8
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

0. (0.010) 1 0 1 1 0 0 1 . 0 0 0 0 . 1 1 0 1 1 . 1 0 . 0 0 0 1 . 1 1 0 0 1 1 0 ( ) 0 1 . 1 1 0 0 1 1 . 1 1 . 1 0 0 . 0 0 0 . 1 1 . 1 0 0 . 0 0 0 1 1 . 1 0 0 0 1 0 0 0 0 .)