Dual Bootstrapped 12 V MOSFET Driver with Output Disable

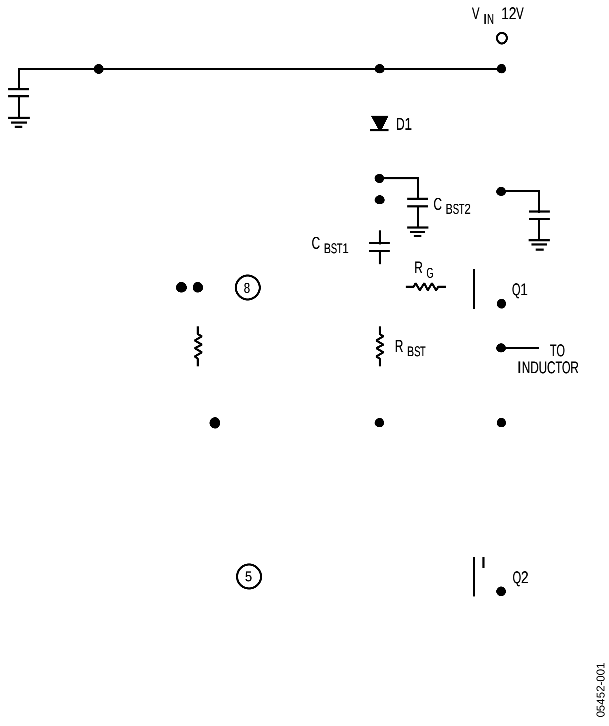
V IN 12V
D1
C BST2
C BST1
R G
Q1
8
R BST
TO INDUCTOR
5
Q2
05452-001

Figure 1.

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[1] F[illegible]-M [illegible] U.S. P[illegible] 6683441.

TABLE OF CONTENTS

[illegible]

REVISION HISTORY

01/08 - Rev 2: Conversion to ON Semiconductor

9/07—Rev. 0 to Rev. A

[illegible]

4/05—Revision 0: Initial Version

SPECIFICATIONS

[illegible]

Table 1.

Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
PWM INPUT						
I -. V .. . H.			2.0			V
I -. V .. . L					0.8	V
I -. C- .. .			J 1		+1	, A
H . . ,			90	250		I V
$\overline{\text{OD}}$ INPUT						
I -. V .. . H.			2.0			V
I -. V .. . L					0.8	V
I -. C- .. .			J 1		+1	, A
H . . ,			90	250		I V
P . .. D . T I ²	- · $\overline{\text{OD}}$	S F. - 3		20	35	
	- $\overline{\text{OD}}$	S F. - 3		40	55	
HIGH-SIDE DRIVER						
O-. -. R . . , S - . . . C- . . .		BST J SW = 12 V		2.2	3.5	_
O-. -. R . . , S . . . C- . .		BST J SW = 12 V		1.0	2.5	_
O-. -. R . . , U . .		BST J SW = 0 V		10		. _
T . . T I	. DRVH	BST J SW = 12 V, C_{LOAD} = 3 F, F. - 4		25	40	
	. DRVH	BST J SW = 12 V, C_{LOAD} = 3 F, F. - 4		20	30	
P . .. D . T I ²	. DRVH	BST J SW = 12 V, C_{LOAD} = 3 F, F. - 4		25	40	
	. DRVH	BST J SW = 12 V, C_{LOAD} = 3 F, F. - 4		25	35	
SW P- .. -D R . .		SW. PGND		10		. _
LOW-SIDE DRIVER						
O-. -. R . . , S - . . . C- . . .				2.0	3.2	_
O-. -. R . . , S . . . C- . .				1.0	2.5	_
O-. -. R . . , U . .		VCC = PGND		10		. _
T . . T I	. DRVL	C_{LOAD} = 3 F, F. - 4		20	35	
	. DRVL	C_{LOAD} = 3 F, F. - 4		16	30	
P . .. D . T I ²	. DRVL	C_{LOAD} = 3 F, F. - 4		12	35	
	. DRVL	C_{LOAD} = 3 F, F. - 4		30	45	
T I -. D .		SW = 5 V	110	190		
		SW = PGND	95	150		
SUPPLY						
S- . V .. . R .	V_{CC}					

ABSOLUTE MAXIMUM RATINGS

TIMING CHARACTERISTICS

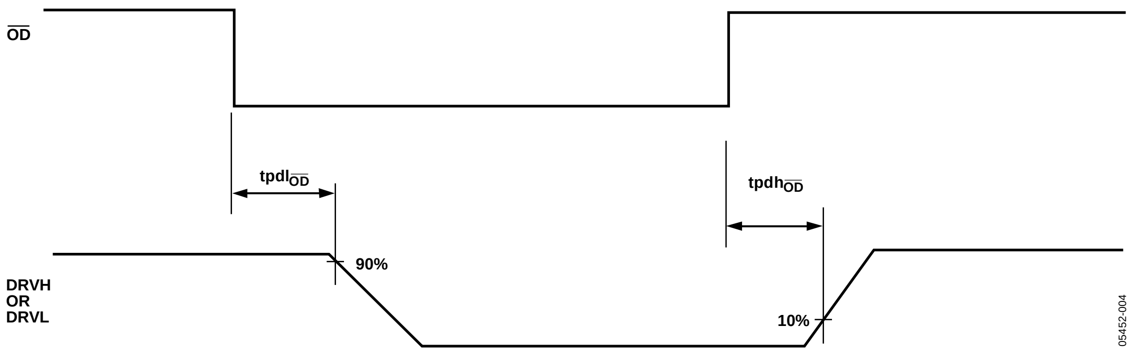
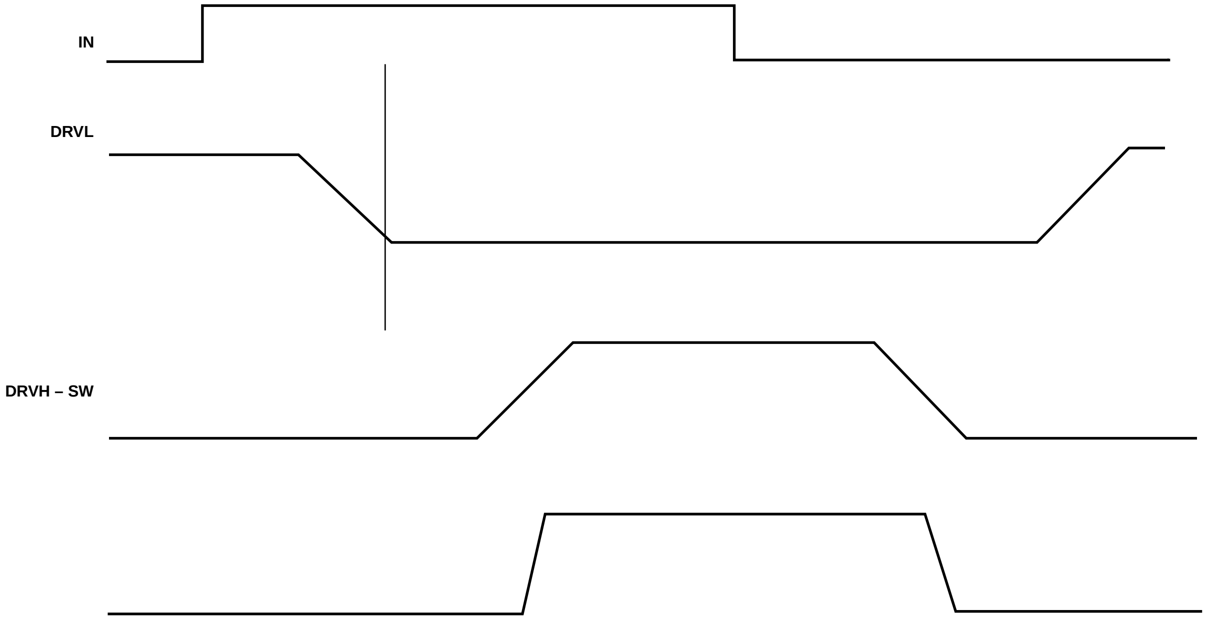
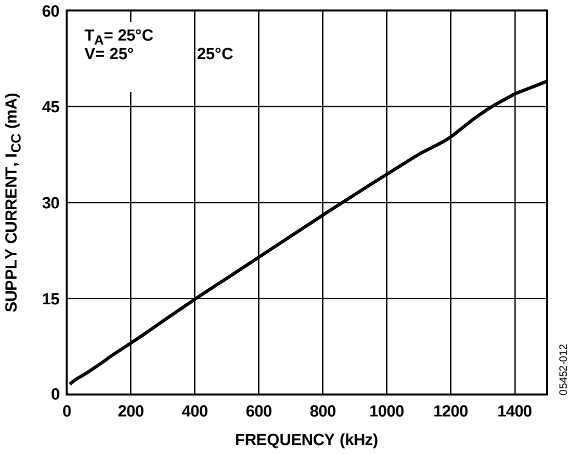

$\overline{OD}$
tpdl$_{\overline{OD}}$
tpdh$_{\overline{OD}}$
90%
DRVH
OR
DRVL
10%
05452-004

Figure 3. Output Disable Timing Diagram


IN
DRVL
DRVH – SW


60
45
30
15
0
0
200
400
600
800
1000
1200
1400
SUPPLY CURRENT, I_{CC} (mA)
FREQUENCY (kHz)
T_A= 25°C
V= 25°
25°C
05452-012

THEORY OF OPERATION

[illegible]

LOW-SIDE DRIVER

[illegible]

HIGH-SIDE DRIVER

[illegible]

[illegible]

[illegible]

OVERLAP PROTECTION CIRCUIT

[illegible]

APPLICATION INFORMATION

SUPPLY CAPACITOR SELECTION

[illegible]

BOOTSTRAP CIRCUIT

[illegible]

$$C_{BST1} \quad C_{BST2} \quad \frac{Q_{GATE}}{V_{GATE}}$$

$$\frac{C_{BST1}}{C_{BST1} \quad C_{BST2}} \quad \frac{V_{GATE}}{V_{CC} \quad V_{D}}$$

[illegible]

Q_{GATE} [illegible]

V_{GATE} [illegible]

V_D [illegible]

[illegible]

$$C_{BST1} \quad \frac{Q_{GATE}}{V_{CC} \quad V_{D}}$$

[illegible]

$$C_{BST2} \quad \frac{Q_{GATE}}{V_{GATE}} \quad C_{BST1}$$

[illegible]

[illegible]

[illegible]

$I_{F(AVG)}$ Q_{GATE} f_{MAX}

[illegible] f_{MAX} [illegible]

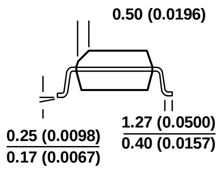
$$I_{MAX} = I_{DC}\ per\ phase + (V_{CC} - V_{OUT}) \times \frac{D_{MAX}}{f_{MAX} \times L_{OUT}}$$

D_{MAX}

L_{OUT}

LOW-SIDE (SYNCHRONOUS) MOSFETS

OUTLINE DIMENSIONS


0.50 (0.0196)
0.25 (0.0098)
0.17 (0.0067)
1.27 (0.0500)
0.40 (0.0157)

COMPLIANT TO JEDEC STANDARDS MS-012-AA

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