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August, 2008 – Rev. 4

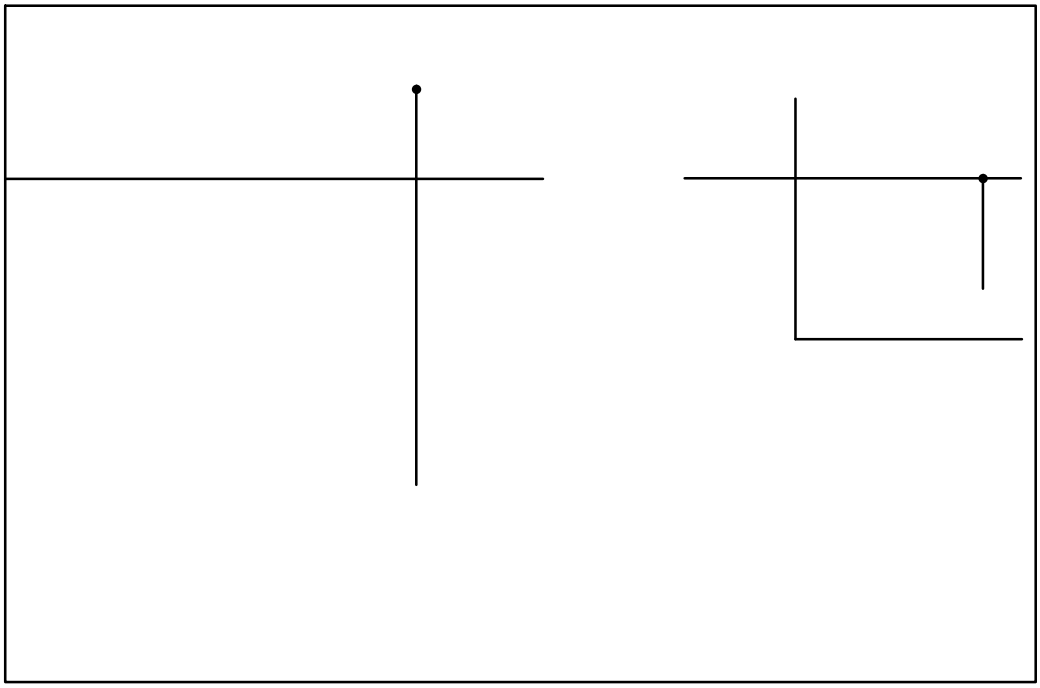


Figure 1. Block Diagram

MAXIMUM RATINGS

Rating		Value	Unit
Operating Ambient Temperature, T_A		0 to 85	°C
Operating Junction Temperature, T_J (Note 1)		0 to 150	°C
Package Thermal Resistance: SO−8 Junction−to−Case, $R_{\theta JC}$ Junction−to−Ambient, $R_{\theta JA}$ (2−Layer Board) Package Thermal Resistance: DFN8 (Note 2) Junction−to−Case, $R_{\theta JC}$ (From die to exposed pad) Junction−to−Ambient, $R_{\theta JA}$		 45 123 7.5 55	 °C/W °C/W °C/W °C/W
Storage Temperature Range, T_S		−65 to 150	°C
Lead Temperature Soldering (10 sec): Reflow (SMD styles only)	Pb−Free (Note 3)	260 peak	°C
JEDEC Moisture Sensitivity Level	SO−8 (260 peak profile)	1	−

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Internally limited by thermal shutdown, 150°C min.
2. 2 layer board, 1 in^2 Cu, 1 oz thickness.
3. 60−180 seconds minimum above 237°C.

NOTE: This device is ESD sensitive. Use standard ESD precautions when handling.

MAXIMUM RATINGS

Pin Symbol	Pin Name	V_{MAX}	V_{MIN}
V_{CC}	Main Supply Voltage Input	15 V	−0.3 V
PGND	Ground	0 V	0 V
BST	Bootstrap Supply Voltage Input	35 V wrt/PGND 40 V < 50 ns wrt/PGND 15 V wrt/SW	−0.3 V wrt/SW
SW	Switching Node (Bootstrap Supply Return)	35 V 40 V < 50 ns	−5.0 V −10 V < 200 ns
DRVH	High−Side Driver Output	BST + 0.3 V	−0.3 V wrt/SW − 2.0 V < 200 ns wrt/SW
DRVL	Low−Side Driver Output	V_{CC} + 0.3 V	−0.3 V DC −5.0 V < 200 ns
IN	DRVH and DRVL Control Input	6.5 V	−0.3 V
$\overline{OD}$	Output Disable	6.5 V	−0.3 V

NOTE: All voltages are with respect to PGND except where noted.

ELECTRICAL CHARACTERISTICS (Note 4) (V_{CC} = 12 V, T_A = 0°C to +85°C, T_J = 0°C to +125°C unless otherwise noted.)

Characteristic	Symbol	Condition	Min	Typ	Max	Unit
Supply						
Supply Voltage Range	V_{CC}	–	4.6	–	13.2	V
Supply Current	I_{SYS}	BST = 12 V, IN = 0 V	–	0.7	5.0	mA
$\overline{OD}$ Input						
Input Voltage High	$V_{\overline{OD}_HI}$	–	2.0	–	–	V
Input Voltage Low	$V_{\overline{OD}_LO}$	–	–	–	0.8	V
Hysteresis		–	–	400	–	mV
Input Current		No internal pullup or pulldown resistors	−1.0	–	+1.0	μA
PWM Input						
Input Voltage High	V_{PWM_HI}	–	2.0	–	–	V
Input Voltage Low	V_{PWM_LO}	–	–	–	0.8	V
Hysteresis	–	–	–	400	–	mV
Input Current	–	No internal pullup or pulldown resistors	−1.0	–	+1.0	μA
High−Side Driver						
Output Resistance, Sourcing Current	–	BST − SW = 12 V	–	2.2	3.4	Ω
Output Resistance, Sinking Current	–	BST − SW = 12 V	–	1.0	1.8	Ω
Output Resistance, Unbiased	–	BST − SW = 0 V	–	15	–	kΩ
Transition Times	t_{rDRVH} t_{fDRVH}	BST − SW = 12 V, C_{LOAD} = 3.0 nF (See Figure 3)	–	20 11	55 45	ns
Propagation Delay Times (Note 5)	$t_{pdhDRVH}$ $t_{pdlDRVH}$	BST − SW = 12 V, C_{LOAD} = 3.0 nF BST − SW = 12 V, C_{LOAD} = 3.0 nF (See Figure 3)	32	45 25		
	$t_{pdl\overline{OD}}$ t_{pdhOD}	(See Figure 2) (See Figure 2)		20 2d		

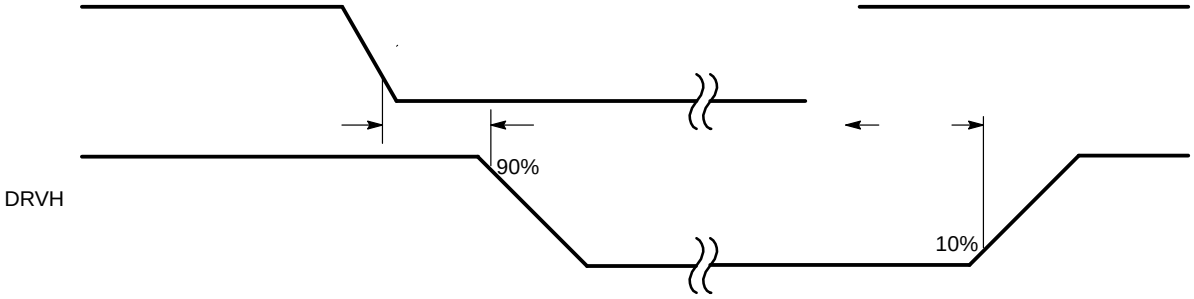
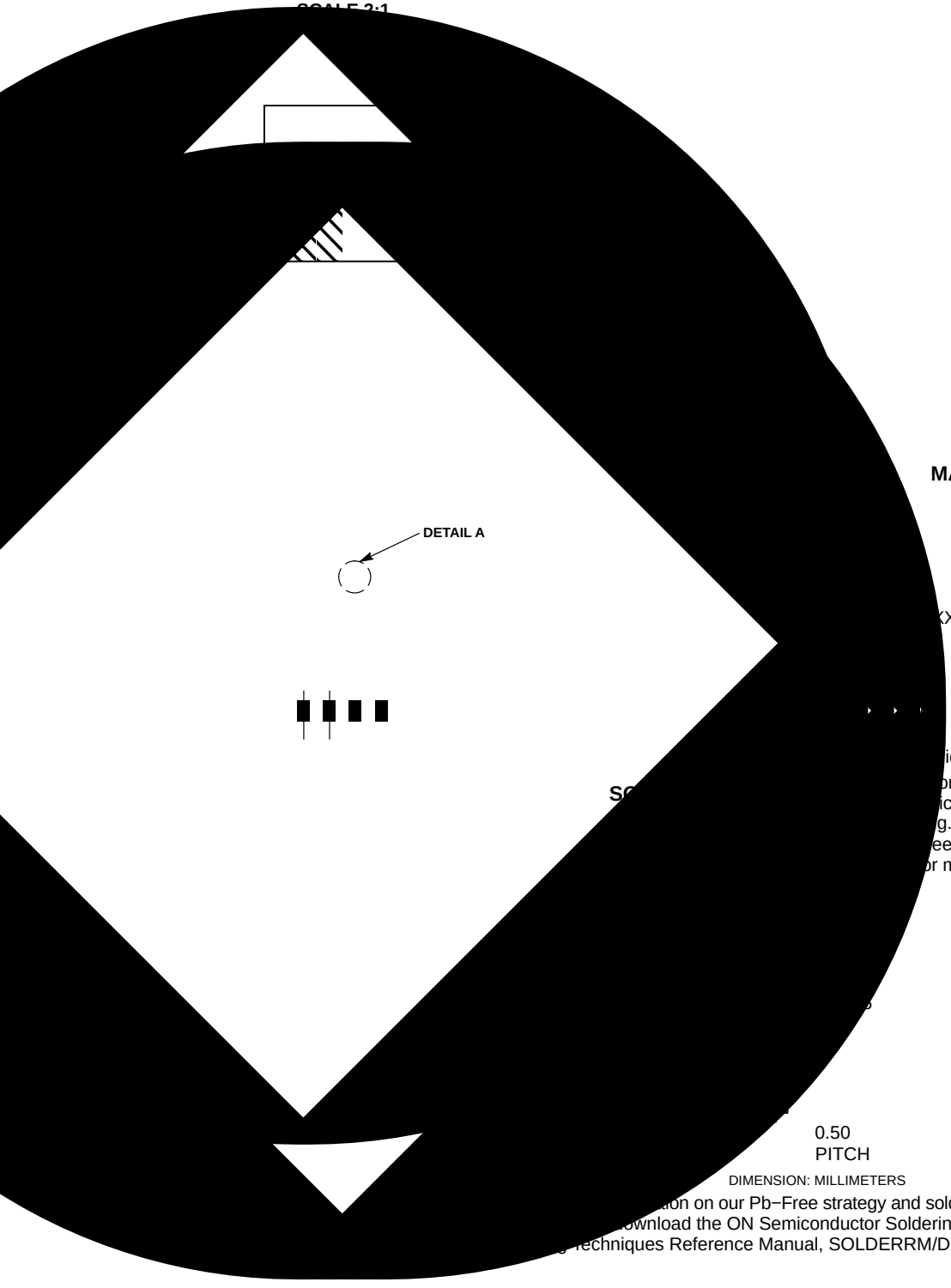


Figure 2. Output Disable Timing Diagram

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

DFN8 3x3, 0.5P
CASE 506BJ−01
ISSUE O

DATE 08 NOV 2007



GENERIC
MARKING DIAGRAM*

8

XXX = Specific Device Code
= Assembly Location
= Wafer Lot
= Year
= Work Week
= Pb−Free Package

icrodot may be in either location)

ormation is generic. Please refer
ice data sheet for actual part
g.

ee indicator, “G” or microdot “ ▪”,
r may not be present.

0.50
PITCH

DIMENSION: MILLIMETERS

tion on our Pb−Free strategy and soldering
ownload the ON Semiconductor Soldering and
Techniques Reference Manual, SOLDERRM/D.

–X–

– – –

⊕	0.	(0.010) Ⓜ	Ⓜ

–Y–

– – –

G

–Z–

C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0	8	0	8
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

0. (0.010) Ⓜ 1 0 1 1 0 0 1 . 0 0 0 0 . 1 1 0 1 1 . 1 0 . 0 0 0 1 . 1 1 0 0 1 1 0 ( ) 0 1 . 1 1 0 0 1 1 . 1 1 . 1 0 0 . 0 0 0 . 1 1 . 1 0 0 . 0 0 . 0 1 1 . 1 0 0 . 0 1 0 0 0 .)

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