Low Cost Microprocessor System Temperature Monitor Microcomputer

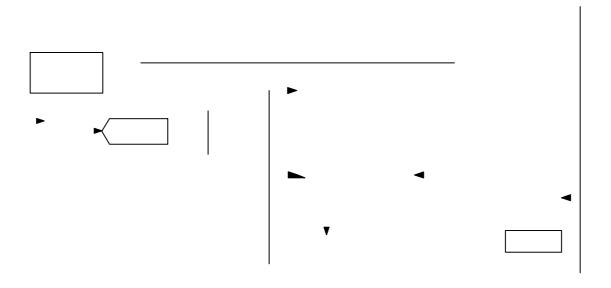


Figure 1. Functional Block Diagram

#### Table 4. ELECTRICAL CHARACTERISTICS (continued)

 $(T_A = T_{MIN} \ to \ T_{MAX}, \ V_{DD} = 3.0 \ V \ to \ 3.6 \ V, \ unless \ otherwise \ noted)$  (Note 1)

Parameter	Test Conditions/Comments		Тур	Max	Unit
SMBus Interface (See Figure 2)				_	
Logic Input High Voltage, V <sub>IH</sub> STBY, SCLK, SDATA	V <sub>DD</sub> = 3.0 V to 5.5 V	2.2	_	_	V
Logic Input Low Voltage, V <sub>IL</sub> STBY, SCLK, SDATA	V <sub>DD</sub> = 3.0 V to 5.5 V	_	_	0.8	V
SMBus Output Low Sink Current	SDATA Forced to 0.6 V	6.0	_	_	mA
ALERT Output Low Sink Current	ALERT Forced to 0.4 V	1.0	_	_	mA
Logic Input Current, I <sub>IH</sub> , I <sub>IL</sub>		-1.0	_	+1.0	μΑ
SMBus Input Capacitance, SCLK, SDATA		-	5.0	-	pF
SMBus Clock Frequency		-	_	100	kHz
SMBus Clock Low Time, t <sub>LOW</sub>	t <sub>LOW</sub> between 10% Points	4.7	-	_	μS
SMBus Clock High Time, t <sub>HIGH</sub>	t <sub>HIGH</sub> between 90% Points	4.0	_	-	μS
SMBus Start Condition Setup Time, tsu:STA		4.7	_	_	μS
SMBus Repeat Start Condition		250	_	_	ns
Setup Time, t <sub>SU:STA</sub>	Between 90% and 90% Points	250	_	-	ns
SMBus Start Condition Hold Time, t <sub>HD:STA</sub>	Time from 10% of SDATA to 90% of SCLK	4.0	-	_	μS
SMBus Stop Condition Setup Time, t <sub>SU:STO</sub>	Time from 90% of SCLK to 10% of SDATA	4.0	-	_	μS
SMBus Data Valid to SCLK	Time for 10% or 90% of SDATA to 10% of SCLK	250	_	-	ns
Rising Edge Time, t <sub>SU:DAT</sub>	Time for 10% or 90% of SDATA to 10% of SCLK	250	_	-	ns
SMBus Data Hold Time, t <sub>BUF:DAT</sub>		0	_	_	μS
SMBus Bus Free Time, t <sub>BUF</sub>	Between Start/Stop Condition	4.7	_	-	μS
SCLK Falling Edge to SDATA		-	_	1	μS
Valid Time, t <sub>VD:DAT</sub>	Master Clocking in Data	-	_	1	μS

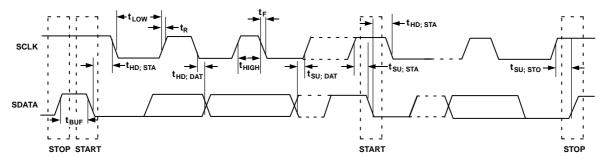


Figure 2. Serial Bus Timing

T<sub>MAX</sub> = 100 C, T<sub>MIN</sub> = 0 C
 Operation at V<sub>DD</sub> = 5.0 V guaranteed by design; not production tested.
 Guaranteed by design; not production tested.

### **TYPICAL PERFORMANCE CHARACTERISTICS**

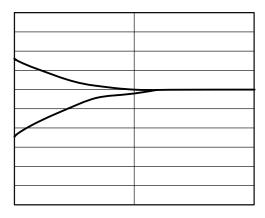


Figure 3. Temperature Error vs. PC Board Track Resistance



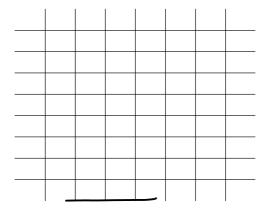


Figure 4. Temperature Error vs. Power Supply **Noise Frequency** 

Figure 5. Temperature Error vs. Common-mode **Noise Frequency** 

Figure 6. Temperature Error vs. Pentium<sup>®</sup> III **Temperature** 

Functional Description		
_		

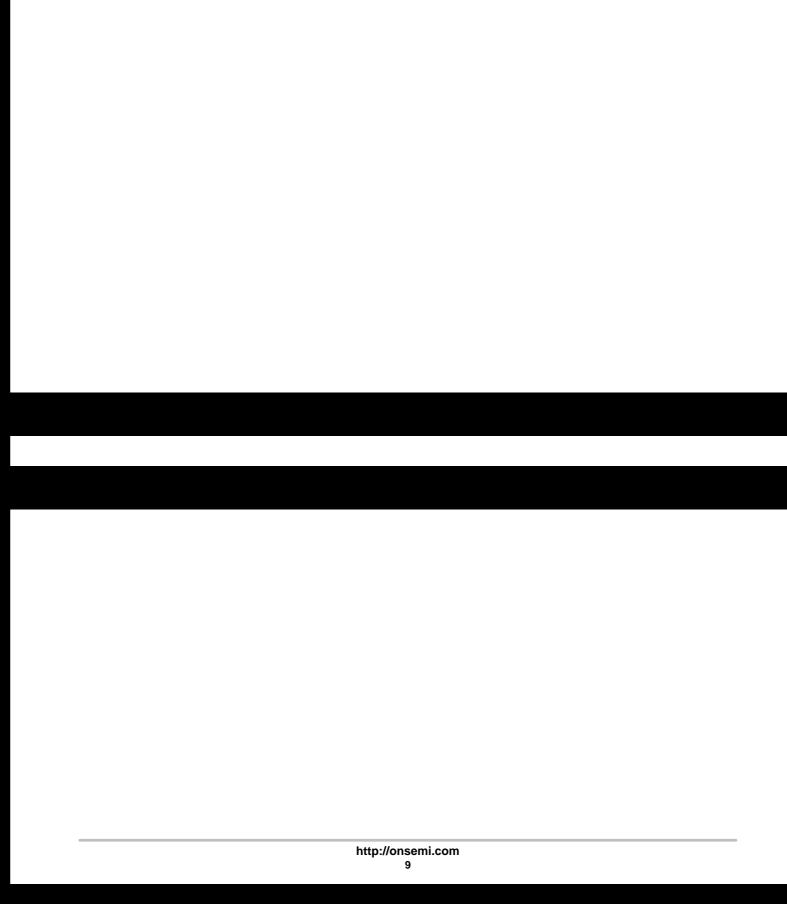


Table 11. DEVICE ADDRESSES (Note 1)

ADD0	ADD1	Device Address
0	0	0011 000
0	NC	0011 001
0	1	0011 010
NC	0	0101 001
NC	NC	0101 010
NC	1	0101 011
1	0	1001 100
1	NC	1001 101
1	1	1001 110

<sup>1.</sup> ADD0 and ADD1 are sampled at powerup only.

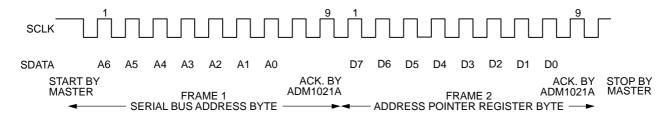


Figure 15. Writing to the Address Pointer Register Only

Low Power Standby Modes	
<u> </u>	
	μ
μ 	

**Sensor Fault Detection** 

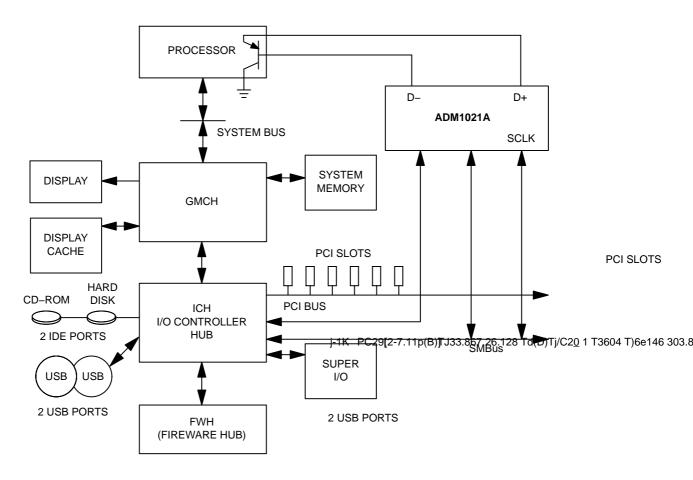
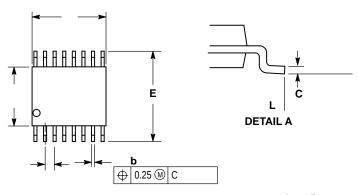


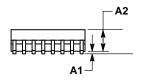
Figure 20. Typical System Using ADM1021A

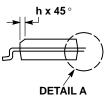


#### **DATE 23 MAR 2011**

#### SCALE 2:1







#### NOTES:

- NOTES:

  1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.

  2. CONTROLLING DIMENSION: MILLIMETERS.

  3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.
- PROTROSION.

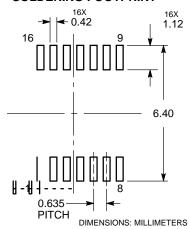
  DIMENSION D DOES NOT INCLUDE MOLD FLASH,
  PROTRUSIONS, OR GATE BURRS. MOLD FLASH,
  PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.005 PER SIDE. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. IN-TERLEAD FLASH OR PROTRUSION SHALL NOT EX-CEED 0.005 PER SIDE. D AND E1 ARE DETERMINED AT DATUM H.

  5. DATUMS A AND B ARE DETERMINED AT DATUM H.

	INC	HES	
DIM	MIN	MAX	
Α	0.053	0.069	
A1	0.004	0.010	
b	0.008	0.012	
С	0.007	0.010	

е	0.025 BSC		
h	0.009	0.020	
L	0.016	0.050	
М	l 0°	l 8°	

#### **SOLDERING FOOTPRINT**



XXXXX = Specific Device Code

ΥY = Year WW = Work Week G = Pb-Free Package

