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November 1992 Revised April 1999

74VHC138 3-to-8 Decoder/Demultiplexer

General Description

The VHC138 is an advanced high speed CMOS 3-to-8 decoder/demultiplexer fabricated with silicon gate CMOS technology. It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

When the device is enabled, 3 binary select inputs (A₀, A₁ and A₂) determine which one of the outputs $(\overline{O}_0-\overline{O}_7)$ will go LOW. When enable input E₃ is held LOW or either \overline{E}_1 or \overline{E}_2 is held HIGH, decoding function is inhibited and all outputs go HIGH.r eil16(r)261

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74VHC138

Truth Table

Inputs				Outputs									
E ₁	E ₂	E ₃	A ₀	A ₁	A ₂	O ₀	01	02	03	04	05	06	07
Н	Х	Х	Х	Х	Х	Н	Н	Н	Н	Н	Н	Н	Н
Х	н	Х	х	х	х	н	н	н	н	н	н	н	н
х	х	L	х	х	х	н	н	н	н	н	н	н	н
L	L	н	L	L	L	L	н	н	н	н	н	н	н
L	L	н	н	L	L	н	L	н	н	н	н	н	н
L	L	н	L	н	L	н	н	L	н	н	н	н	н
L	L	Н	н	н	L	н	н	н	L	н	н	н	н
L	L	н	L	L	н	н	н	н	н	L	н	н	н
L	L	н	н	L	н	н	н	н	н	н	L	н	н
L	L	н	L	н	н	н	н	н	н	н	н	L	н
L	L	н	н	н	н	н	н	н	н	н	н	н	L

H = HIGH Voltage Level L = LOW Voltage Level X = Immaterial

Absolute Maximum Ratings(Note 1)

 $\label{eq:supply_voltage} \begin{array}{l} {\rm Supply \ Voltage \ }({\rm V_{CC}}) \\ {\rm DC \ Input \ Voltage \ }({\rm V_{IN}}) \\ {\rm DC \ Output \ Voltage \ }({\rm V_{OUT}}) \\ {\rm Input \ Diode \ Co \ 1 \ TP-17d} \end{array}$

-0.5V to +7.0V -0.5V to +7.0V -0.5V to V_{CC} + 0.5V

Recommended Operating

Conditions (Note 2)

Note 1: Absolute Maximum Ratings are values beyond which the device may be damaged or have its useful life impaired. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation outside databook specifications.

Note 2: Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

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Symbol	Parameter	V _{CC} (V)	$T_A = 25^{\circ}C$			$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$		Unite	Conditions
			Min	Тур	Max	Min	Max	Units	Conditions
t _{PLH}	Propagation Delay	$\textbf{3.3}\pm\textbf{0.3}$		8.2	11.4	1.0	13.5		$C_L = 15 \text{ pF}$
t _{PHL}	A_n to \overline{O}_n			10.0	15.8	1.0	18.0	ns	$C_L = 50 \text{ pF}$
		5.0 ± 0.5		5.7	8.1	1.0	9.5	200	$C_L = 15 \text{ pF}$
				7.2	10.1	1.0	11.5	115	$C_L = 50 \text{ pF}$
t _{PLH}	Propagation Delay	$\textbf{3.3}\pm\textbf{0.3}$		8.1	12.8	1.0	15.0	200	$C_L = 15 \text{ pF}$
t _{PHL}	E_3 to \overline{O}_n			10.6	16.3	1.0	18.5	115	C _L = 50 pF
		5.0 ± 0.5		5.6	8.1	1.0	9.5	ne	$C_L = 15 \text{ pF}$
				7.1	10.1	1.0	11.5	113	C _L = 50 pF
t _{PLH}	Propagation Delay	3.3 ± 0.3		8.2	11.4	1.0	13.5	200	C _L = 15 pF
t _{PHL}	\overline{E}_1 or \overline{E}_2 to \overline{O}_n			10.7	14.9	1.0	17.0	115	$C_L = 50 \text{ pF}$
		5.0 ± 0.5		5.8	8.1	1.0	9.5	ne	$C_L = 15 \text{ pF}$
				7.3	10.1	1.0	11.5	113	$C_L = 50 \text{ pF}$
C _{IN}	Input Capacitance			4	10		10	pF	V _{CC} = Open
C _{PD}	Power Dissipation			34				pF	(Note 3)
	Capacitance								

Note 3: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC} (opr.) = $C_{PD} * V_{CC} * f_{IN} + I_{CC}$.

74VHC138

16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Package Number M16A

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Physical Dimensions

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