

74VHC138 3-to-8 Decoder/Demultiplexer

General Description

The VHC138 is an advanced high speed CMOS 3-to-8 decoder/demultiplexer fabricated with silicon gate CMOS technology. It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

When the device is enabled, 3 binary select inputs (A_0 , A_1 and A_2) determine which one of the outputs (\overline{O}_0 – \overline{O}_7) will go LOW. When enable input E_3 is held LOW or either \overline{E}_1 or \overline{E}_2 is held HIGH, decoding function is inhibited and all outputs go HIGH. r eil16(r)261

Truth Table

Inputs						Outputs							
\overline{E}_1	\overline{E}_2	E_3	A_0	A_1	A_2	\overline{O}_0	\overline{O}_1	\overline{O}_2	\overline{O}_3	\overline{O}_4	\overline{O}_5	\overline{O}_6	\overline{O}_7
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial

Absolute Maximum Ratings (Note 1)

Supply Voltage (V_{CC})	-0.5V to +7.0V
DC Input Voltage (V_{IN})	-0.5V to +7.0V
DC Output Voltage (V_{OUT})	-0.5V to $V_{CC} + 0.5V$
Input Diode Co 1 TP-17d	

Recommended Operating Conditions (Note 2)

Note 1: Absolute Maximum Ratings are values beyond which the device may be damaged or have its useful life impaired. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation outside databook specifications.

Note 2: Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

AC Electrical Characteristics

Symbol	Parameter	V _{CC} (V)	T _A = 25°C			T _A = -40°C to +85°C		Units	Conditions
			Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay A _n to \overline{O}_n	3.3 ± 0.3	8.2	11.4	1.0	13.5	ns	C _L = 15 pF	
t _{PHL}			10.0	15.8	1.0	18.0		C _L = 50 pF	
		5.0 ± 0.5	5.7	8.1	1.0	9.5	ns	C _L = 15 pF	
			7.2	10.1	1.0	11.5		C _L = 50 pF	
t _{PLH}	Propagation Delay E ₃ to \overline{O}_n	3.3 ± 0.3	8.1	12.8	1.0	15.0	ns	C _L = 15 pF	
t _{PHL}			10.6	16.3	1.0	18.5		C _L = 50 pF	
		5.0 ± 0.5	5.6	8.1	1.0	9.5	ns	C _L = 15 pF	
			7.1	10.1	1.0	11.5		C _L = 50 pF	
t _{PLH}	Propagation Delay \overline{E}_1 or \overline{E}_2 to \overline{O}_n	3.3 ± 0.3	8.2	11.4	1.0	13.5	ns	C _L = 15 pF	
t _{PHL}			10.7	14.9	1.0	17.0		C _L = 50 pF	
		5.0 ± 0.5	5.8	8.1	1.0	9.5	ns	C _L = 15 pF	
			7.3	10.1	1.0	11.5		C _L = 50 pF	
C _{IN}	Input Capacitance		4	10		10	pF	V _{CC} = Open	
C _{PD}	Power Dissipation Capacitance		34				pF	(Note 3)	

Note 3: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC (opr.)} = C_{PD} * V_{CC} * f_{IN} + I_{CC}.

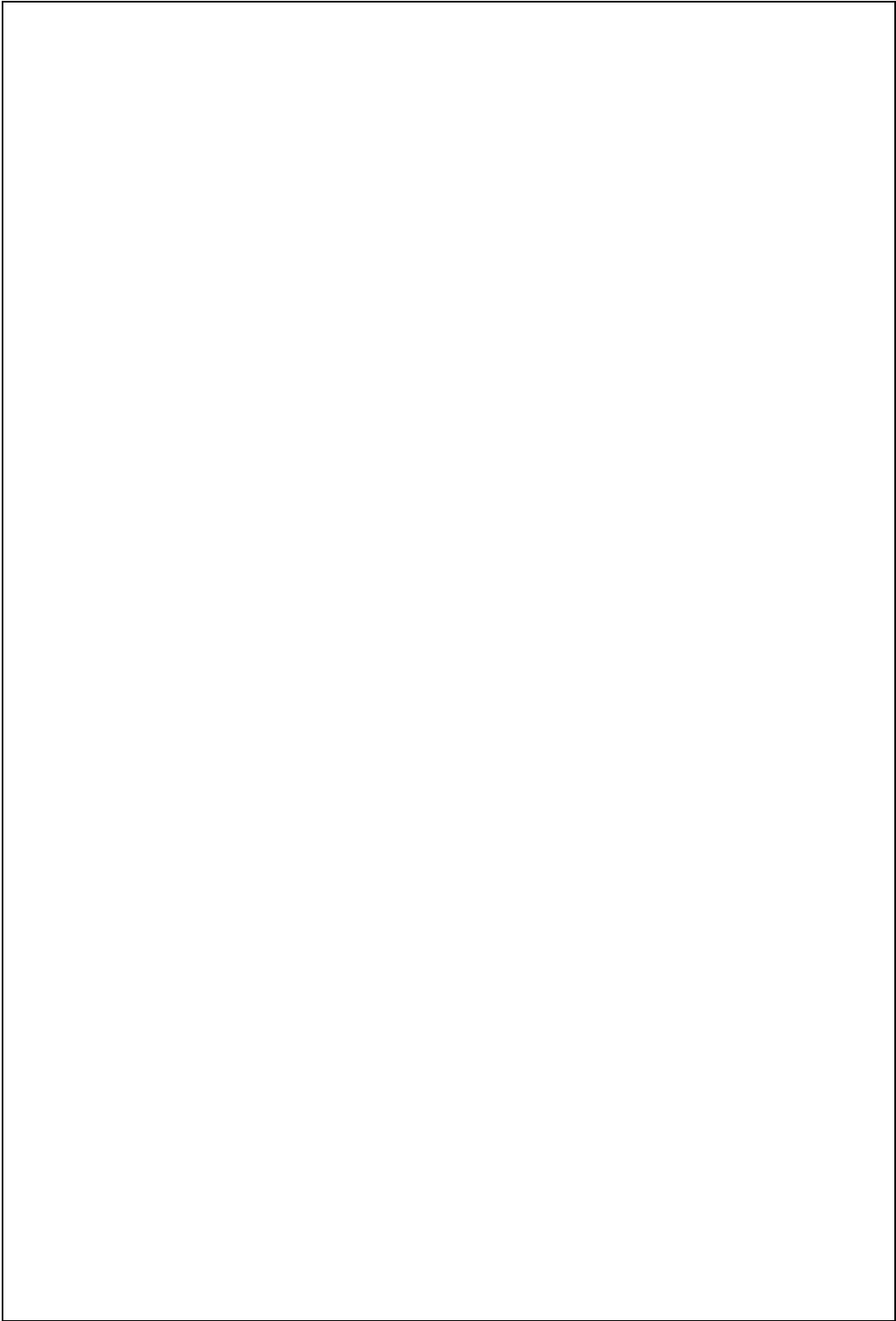
Physical Dimensions inches (millimeters) unless otherwise noted

74VHC138

**16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M16A**

74VHC138

Physical Dimensions



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