

General Description

The VHC112 is an advanced high speed CMOS device fabricated with silicon gate CMOS technology. It achieves the high-speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

The VHC112 contains two independent, high-speed JK flip-flops with Direct Set and Clear inputs. Synchronous state changes are initiated by the falling edge of the clock. Triggering occurs at a voltage level of the clock and is not directly related to transition time. The J and K inputs can change when the clock is in either state without affecting the flip-flop, provided that they are in the desired state during the recommended setup and hold times relative to the falling edge of the clock. The LOW signal on PR or CLR prevents clocking and forces Q and \bar{Q} HIGH, respectively. Simultaneous LOW signals on PR and CLR force both Q and \bar{Q} HIGH.

An input protection circuit ensures that 0 V to 5.5 V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5 V to 3 V systems and two supply systems such as battery backup. This circuit prevents device destruction due to mismatched supply and input voltages.

Features

- High Speed: $f_{MAX} = 200$ MHz (Typ.) at $V_{CC} = 5.0$ V
- Low Power Dissipation: $I_{CC} = 2$ μ A (Max.) at $T_A = 25^\circ$ C
- High Noise Immunity: $V_{NIH} = V_{NIL} = 28\%$ V_{CC} (Min.)
- Power Down Protection is Provided on All Inputs
- Pin and Function Compatible with 74HC112
- These are Pb-Free Devices

MARKING DIAGRAM

See detailed ordering and shipping information on page 5 of this data sheet.

74VHC112

Connection Diagram

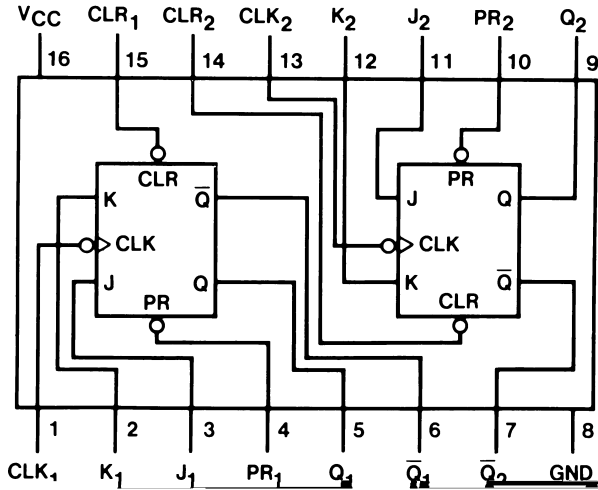


Figure 1. Connection Diagram

TRUTH TABLE

Input					Outputs	
PR	CLR	$\bar{C}P$	J	K	Q	\bar{Q}
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H	H
H	H	\sim	h	h	\bar{Q}_0	Q ₀
H	H	\sim	l	h	L	H
H	H	\sim	h	l	H	L
HCLR						

PIN DESCRIPTION

Pin Names	Description
J ₁ , J ₂ , K ₁ , K ₂	Data Inputs
CLK ₁ , CLK ₂	Clock Pulse Inputs (Active Falling Edge)
CLR ₁ , CLR ₂	Direct Clear Inputs (Active LOW)
PR ₁ , PR ₂	Direct Preset Inputs (Active LOW)
Q ₁ , Q ₂ , \bar{Q}_1 , \bar{Q}_2	Outputs

74VHC112

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	-0.5 to +6.5	V
V_{IN}	DC Input Voltage	-0.5 to +6.5	V
V_{OUT}	DC Output Voltage	-0.5 to $V_{CC} + 0.5$	

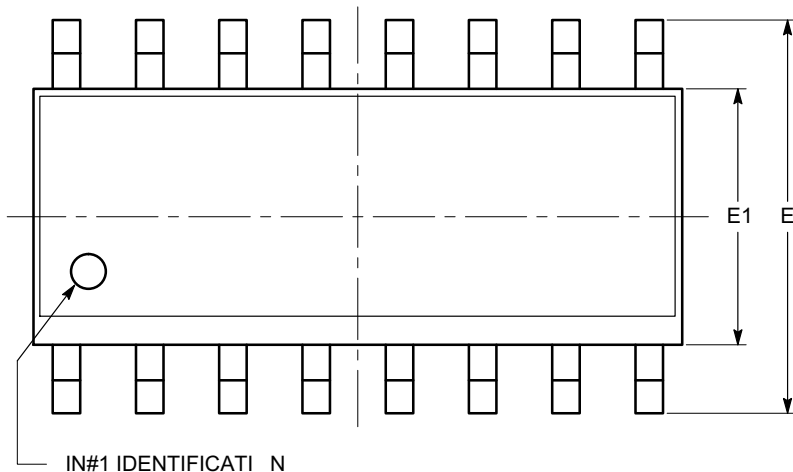
74VHC112

AC ELECTRICAL CHARACTERISTICS

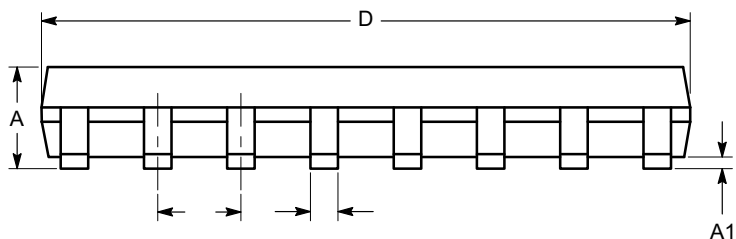
Symbol	Parameter	Conditions	V _{CC} (V)	T _A = 25°C	T _A = -40
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SOIC-16, 150 mils
CASE 751BG-01
ISSUE O

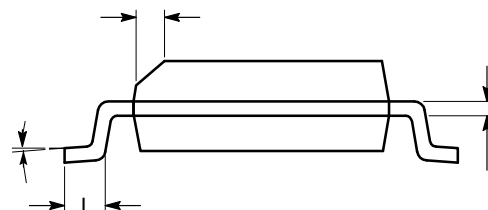
DATE 19 DEC 2008



TOP VIEW



SIDE VIEW



END VIEW

Notes:

- (1) All dimensions are in millimeters. All dimensions are in millimeters.
- (2) Compliance with JEDEC MS-012.

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DESCRIPTION:	SOIC-16, 150 MILS	PAGE 1 OF 1

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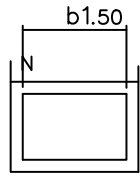
TSSOP 16

SEE DETAIL "A"

0.19

0.09

4.30

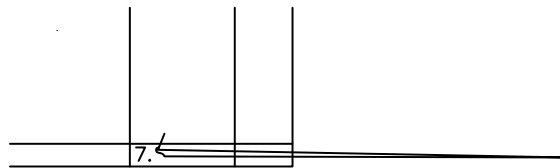


COMMON DIMENSIONS
 NOM. MAX.
 ——— 1.10
 ——— 0.15

A₂
 b
 b1
 c
 c1
 D
 E1
 C
 E
 L

SEE VA

0.65 BSC
 6.40 BSC
 | 0.60 | 0.70



UNITS IN MILLIMETERS

SEE VARIATIONS
 | ——— | 8°

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