4 112

General Description

The VHC112 is an advanced high speed CMOS device fabricated with silicon gate CMOS technology. It achieves the high−speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

The VHC112 contains two independent, high−speed JK flip−flops with Direct Set and Clear inputs. Synchronous state changes are initiated by the falling edge of the clock. Triggering occurs at a voltage level of the clock and is not directly related to transition time. The J and K inputs can change when the clock is in either state without affecting the flip−flop, provided that they are in the desired state during the recommended setup and hold times relative to the falling edge of the clock. The LOW signal on PR or CLR prevents clocking and forces Q and $\overline{Q}$ HIGH, respectively. Simultaneous LOW signals on PR and CLR force both Q and $\overline{Q}$ HIGH.

An input protection circuit ensures that 0 V to 5.5 V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5 V to 3 V systems and two supply systems such as battery backup. This circuit prevents device destruction due to mismatched supply and input voltages.

Features

- High Speed: f_{MAX} = 200 MHz (Typ.) at V_{CC} = 5.0 V
- Low Power Dissipation: I_{CC} = 2 μA (Max.) at T_A = 25°C
- High Noise Immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC} (Min.)
- Power Down Protection is Provided on All Inputs
- Pin and Function Compatible with 74HC112
- These are Pb−Free Devices

MARKING DIAGRAM

See detailed ordering and shipping information on page 5 of this data sheet.

Connection Diagram

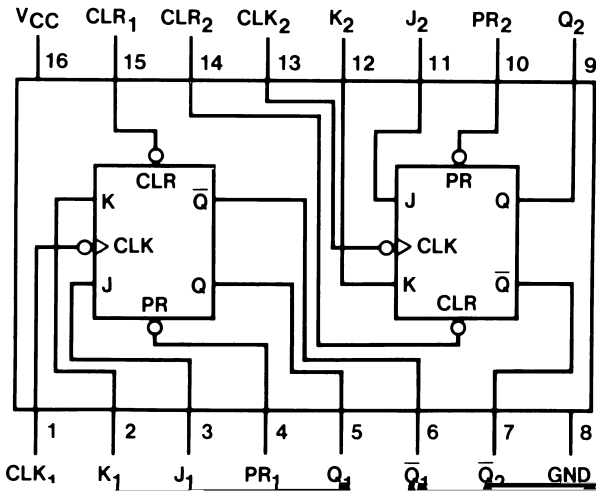


Figure 1. Connection Diagram

PIN DESCRIPTION

Pin Names	Description
J_1, J_2, K_1, K_2	Data Inputs
CLK_1, CLK_2	Clock Pulse Inputs (Active Falling Edge)
CLR_1, CLR_2	Direct Clear Inputs (Active LOW)
PR_1, PR_2	Direct Preset Inputs (Active LOW)
Q_1, Q_2, $\overline{Q}_1$, $\overline{Q}_2$	Outputs

TRUTH TABLE

Input					Outputs	
PR	**CLR**	**$\overline{CP}$**	**J**	**K**	**Q**	**$\overline{Q}$**
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H	H
H	H	⌥	h	h	$\overline{Q}_0$	Q_0
H	H	⌥	l	h	L	H
H	H	⌥	h	l	H	L

HCLR

ABSOLUTE MAXIMUM RATINGS

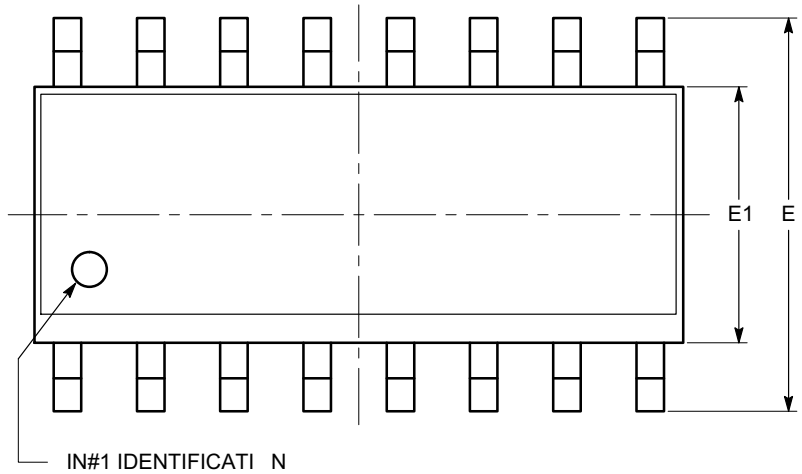
Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	−0.5 to +6.5	V
V_{IN}	DC Input Voltage	−0.5 to +6.5	V
V_{OUT}	DC Output Voltage	−0.5 to V_{CC} + 0.5	

AC ELECTRICAL CHARACTERISTICS

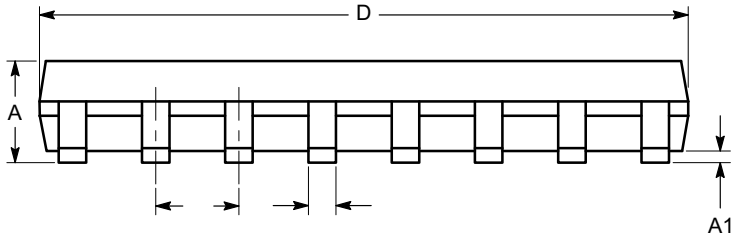
Symbol	Parameter	Conditions	V_{CC} (V)	T_A = 25°C	T_A = −40

SOIC−16, 150 mils
CASE 751BG−01
ISSUE O

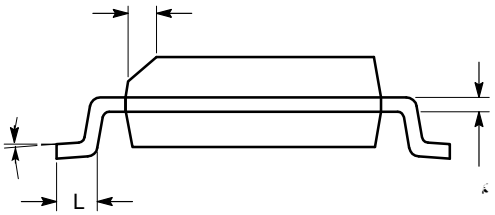
DATE 19 DEC 2008



TOP VIEW



SIDE VIEW

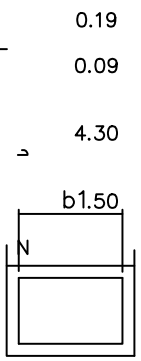


END VIEW

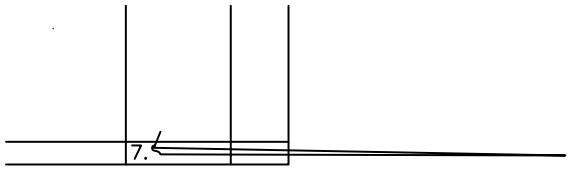
Notes:
(1) A [illegible] n [illegible] na [illegible] n m [illegible] m [illegible] . An [illegible] n [illegible] .
(2) C [illegible] JEDEC MS-012.

DOCUMENT NUMBER:	**98AON34275E**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**SOIC−16, 150 MILS**	**PAGE 1 OF 1**

TSSOP 16



	COMMON DIMENSIONS NOM.	MAX.
A_2		1.10
b		0.15
b1		
c		
c1		
D	SEE VA	
E1		
e	0.65 BSC	
E	6.40 BSC	
L	0.60	0.70
	SEE VARIATIONS	
	—	8°



ONS IN MILLIMETERS

MOLD FLASH OR PROTR