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Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain

March 2000
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74VCX164245

Low Voltage 16-Bit Dual Supply Translating Transceiver with 3-STATE Outputs

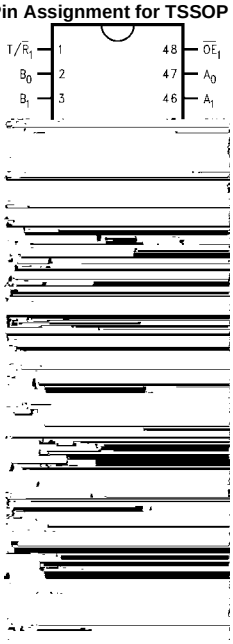
General Description

The VCX164245 is a dual supply, 16-bit translating transceiver that is designed for two way asynchronous communication between busses at different supply voltages by providing true signal translation. The supply rails consist of V_{CCB}, which is the higher potential rail operating at 2.3V to 3.6V and V_{CCA}, which is the lower potential rail operating at 1.65V to 2.7V. (V_{CCA} must be less than or equal to V_{CCB} for proper device operation.) This dual supply design allows for translation from 1.8V to 2.5V busses to busses at a higher potential, up to 3.3V.

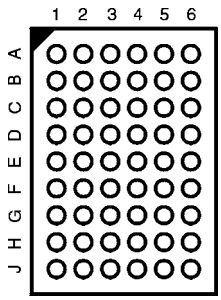
The Transmit/Receive ($T/\overline{R}$) input determines the direction of data flow. Transmit (active-HIGH) enables data from A Ports to B Ports. R

Connection Diagrams

Pin Assignment for TSSOP



Pin Assignment for FBGA



(Top Through View)

Pin Descriptions

Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active LOW)
$T/\overline{R}_n$	Transmit/Receive Input
A_0–A_{15}	Side A Inputs or 3-STATE Outputs
B_0–B_{15}	Side B Inputs or 3-STATE Outputs
NC	No Connect

FBGA Pin Assignments

	1	2	3	4	5	6
A	B_0	NC	$T/\overline{R}_1$	$\overline{OE}_1$	NC	A_0
B	B_2	B_1	NC	NC	A_1	A_2
C	B_4	B_3	V_{CCB}	V_{CCA}	A_3	A_4
D	B_6	B_5	GND	GND	A_5	A_6
E	B_8	B_7	GND	GND	A_7	A_8
F	B_{10}	B_9	GND	GND	A_9	A_{10}
G	B_{12}	B_{11}	V_{CCB}	V_{CCA}	A_{11}	A_{12}
H	B_{14}	B_{13}	NC	NC	A_{13}	A_{14}
J	B_{15}	NC	$T/\overline{R}_2$	$\overline{OE}_2$	NC	A_{15}

Truth Tables

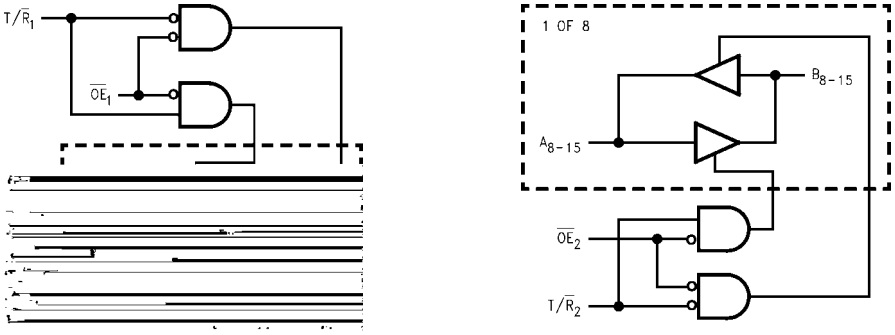
Inputs		Outputs
$\overline{OE}_1$	$T/\overline{R}_1$	
L	L	Bus B_0–B_7 Data to Bus A_0–A_7
L	H	Bus A_0–A_7 Data to Bus B_0–B_7

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial (HIGH or LOW, inputs may not float)
Z = High Impedance

Translator Power Up Sequence Recommendations

To guard against power up problems, some simple guidelines need to be adhered to. The VCX164245 is designed so that the control pins ($T/\overline{R}_n$, $\overline{OE}_n$) are supplied by V_{CCB}. Therefore the first recommendation is to begin by powering up the control side of the device, V_{CCB}. The $\overline{OE}_n$ control pins should be ramped with or ahead of V_{CCB}, this will guard against bus contentions and oscillations as all A Port and B Port outputs will be disabled. To ensure the high impedance state during power up or power down, $\overline{OE}_n$ should be tied to V_{CCB} through a pull up resistor. The minimum value of the resistor is determined by the current sourcing capability of the driver. Second, the $T/\overline{R}_n$ control pins should be placed at logic low (0V) level, this will ensure that the B-side bus pins are configured as inputs to help guard against bus contention and oscillations. B-side Data Inputs should be driven to a valid logic level (0V or V_{CCB}), this will prevent excessive current draw and oscillations. V_{CCA} can then be powered up after V_{CCB}, but should never exceed the V_{CCB} voltage level. Upon completion of these steps the device can then be configured for the users desired operation. Following these steps will help to prevent possible damage to the translator device as well as other system components.

Logic Diagrams



Please note that these diagrams are provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings(Note 4)

Supply Voltage	
V_{CCA}	−0.5V to V_{CCB}
V_{CCB}	−0.5V to 4.6V
DC Input Voltage (V_I)	−0.5V to +4.6V
DC Output Voltage ($V_{I/O}$)	
Outputs 3-STATE	−0.5V to +4.6V
Outputs Active (Note 5)	
An	−0.5V to V_{CCA} + 0.5V
Bn	−0.5V to V_{CCB} + 0.5V
DC Input Diode Current (I_{IK})	
V_I < 0V	−50 mA
DC Output Diode Current (I_{OK})	
V_O < 0V CCA 0V	

Recommended Operating Conditions (Note 6)

Note 4: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 5: I_O Absolute Maximum Rating must be observed.

Note 6: Unused inputs or I/O pins must be held HIGH or LOW. They may not float.

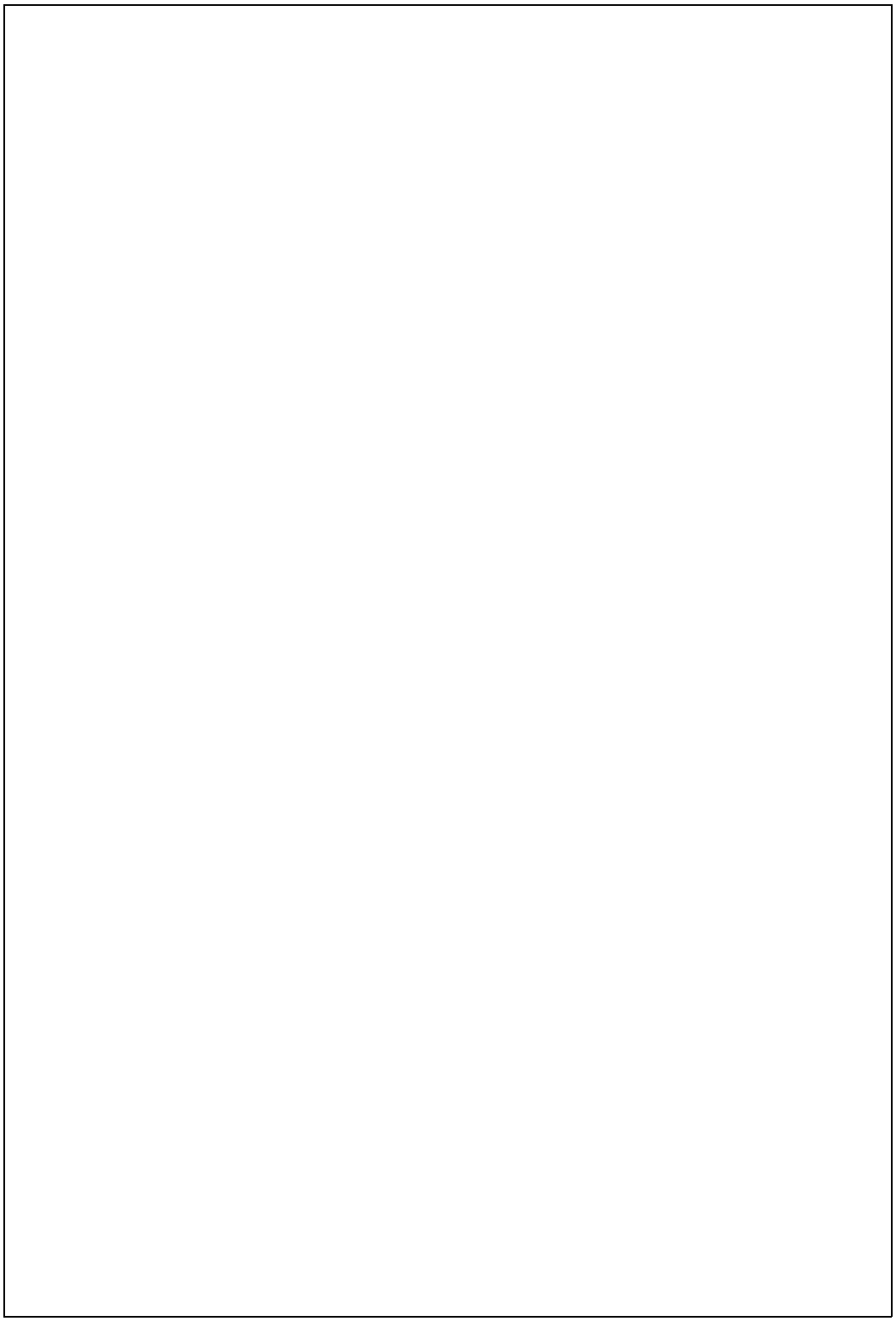
Note 7: Operation requires: $V_{CCA} \leq V_{CCB}$

DC Electrical Characteristics ($1.65V < V_{CCA} \leq 1.95V$, $2.3V < V_{CCB} \leq 2.7V$)

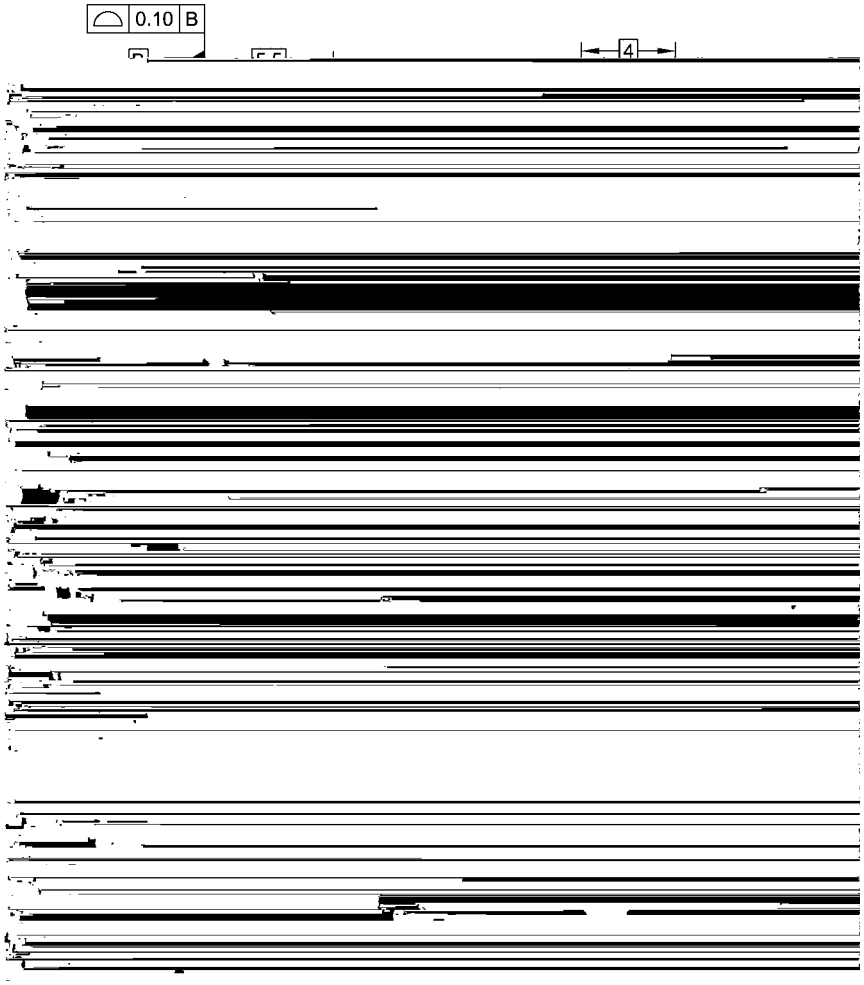
DC Electrical Characteristics (1.65V

AC Electrical Characteristics

Note 8: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{osHL}) or LOW-to-HIGH (t_{osLH}).



Physical Dimensions inches (millimeters) unless otherwise noted



54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide
Package Number BGA54A