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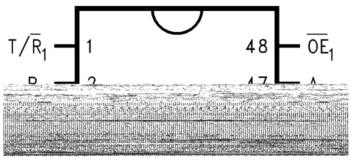
May 2007

74VCX163245
Low Voltage 16-Bit Dual Supply Translating Transceiver with 3-STATE Outputs

Features

Connection Diagram

Pin Assignment for TSSOP



Pin Assignment for FBGA

(Top Thru View)

FBGA Pin Assignments

	1	2	3	4	5	6
A	B_0	NC	T/$\overline{R}_1$	$\overline{OE}_1$	NC	A_0
B	B_2	B_1	NC	NC	A_1	A_2
C	B_4	B_3	V_{CCB}	V_{CCA}	A	

Pin Descriptions

Logic Diagram

Truth Tables

Inputs		
$\overline{OE}_1$	$T/\overline{R}_1$	Outputs
L	L	Bus B_0–B_7 Data to Bus A_0–A_7
L	H	Bus gU7 9 rn70.4944 0 TD 0.2164 Tw (must bta to (2us Tf 10 0)Tj 0 0 0 1 8l1 538 rntar944 0 TD 0.216 Tw (must

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial (HIGH or LOW, inputs may not float)

Z = High Impedance

VCX163245 Translator Power Up Sequence Recommendations

To guard against power up problems, some simple guidelines need to be adhered to. The VCX163245 is designed so that the control pins ($T/\overline{R}_n$, $\overline{OE}_n$) are supplied by V_{CCB}. Therefore the first recommendation is to begin by powering up the control side of the device, V_{CCB}. The $\overline{OE}_n$ control pins should be ramped with or ahead of V_{CCB}, this will guard against bus contentions and oscillations as all A Port and B Port outputs will be disabled. To ensure the high impedance state during power up or power down, $\overline{OE}_n$ should be tied to V_{CCB} through a pull up resistor. The minimum value of the resistor is determined by the current sourcing capability of the driver. Second, the $T/\overline{R}_n$ control pins should be placed at logic LOW (0V) level, this will ensure that the B-side bus pins are configured as inputs to help guard against bus contention and oscillations. B-side Data Inputs should be driven to a valid logic level (0V or V_{CCB}), this will prevent excessive current draw and oscillations. V_{CCA} can then be powered up after V_{CCB}, however V_{CCA} must be greater than or equal to V_{CCB} to ensure proper device operation. Upon completion of these steps the device can then be configured for the users desired operation. Following these steps will help to prevent possible damage to the translator device as well as other system components.

Logic Diagrams

Please note that these diagrams are provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Electrical Characteristics (1.65V < V_{CCB} ≤ 1.95V, 2.3V < V_{CCA} ≤ 2.7V)

Symbol	Parameter		V_{CCB} (V)	V_{CCA} (V)	Conditions	Min.	Max.	Units
V_{IHA}	HIGH Level Input Voltage	A_n	1.65–1.95	2.3–2.7		1.6		V
V_{IHB}		B_n, T/$\overline{R}$, $\overline{OE}$	1.65–1.95	2.3–2.7		0.65 x V_{CCB}		V
V_{ILA}	LOW Level Input Voltage	A_n	1.65–1.95	2.3–2.7			0.7	V
V_{ILB}		B_n, T/$\overline{R}$, $\overline{OE}$	1.65–1.95	2.3–2.7			0.35 x V_{CCB}	V
V_{OHA}	HIGH Level Output Voltage		1.65–1.95	2.3–2.7	I_{OH} = –100µA	V_{CCA} – 0.2		V
			1.65	2.3–2.7	I_{OH} = –18mA	1.7		
V_{OHB}	HIGH Level Output Voltage		1.65–1.95	2.3–2.7	I_{OH} = –100µA	V_{CCB} – 0.2		V
			1.65–1.95	2.3	I_{OH} = –6mA	1.25		
V_{OLA}	Low Level Output Voltage		1.65–1.95	2.3–2.7	I_{OL} = 100µA		0.2	V
			1.65	2.3–2.7	I_{OL} = 18mA		0.6	
V_{OLB}	Low Level Output Voltage		1.65–1.95	2.3–2.7	I_{OL} = 100µA		0.2	V
			1.65–1.95	2.3	I_{OL} = 6mA		0.3	
I_I	Input Leakage Current @ $\overline{OE}$, T/$\overline{R}$		1.65–1.95	2.3–2.7	0V ≤ V_I ≤ 3.6V		±5.0	µA
I_{OZ}	3-STATE Output Leakage		1.65–1.95	2.3–2.7	0V ≤ V_O ≤ 3.6V, $\overline{OE}$ = V_{CCB}, V_I = V_{IH} or V_{IL}		±10	µA
I_{OFF}	Power Off Leakage Current		0	0	0 ≤ (V_I, V_O) ≤ 3.6V		10	µA
I_{CCA} / I_{CCB}	Quiescent Supply Current, per supply, V_{CCA} / V_{CCB}		1.65–1.95	2.3–2.7	A_n = V_{CCA} or GND, B_n, $\overline{OE}$, & T/$\overline{R}$ = V_{CCB} or GND		20	µA
			1.65–1.95	2.3–2.7	V_{CCA} ≤ An ≤ 3.6V, V_{CCB} ≤ B_n, $\overline{OE}$, T/$\overline{R}$ ≤ 3.6V		±20	µA
ΔI_{CC}	Increase in I_{CC} per Input, B_n, T/$\overline{R}$, $\overline{OE}$		1.65–1.95	2.3–2.7	V_I = V_{CCB} – 0.6V		750	µA
	Increase in I_{CC} per Input, A_n							

DC Electrical Characteristics (1.65V < V_{CCB} ≤ 1.95V, 3.0V < V_{CCA} ≤ 3.6V)

Symbol	Parameter		V_{CCB} (V)	V_{CCA} (V)	Conditions	Min.	Max.	Units
V_{IHA}	HIGH Level Input Voltage	A_n	1.65–1.95	3.0–3.6		2.0		V
V_{IHB}		B_n, T/$\overline{R}$, $\overline{OE}$	1.65–1.95	3.0–3.6		0.65 x V_{CCB}		V
V_{ILA}	LOW Level Input Voltage	A_n	1.65–1.95	3.0–3.6			0.8	V
V_{ILB}		B_n, T/$\overline{R}$, $\overline{OE}$	1.65–1.95	3.0–3.6			0.35 x V_{CCB}	V
V_{OHA}	HIGH Level Output Voltage		1.65–1.95	3.0–3.6	I_{OH} = –100µA	V_{CCA} – 0.2		V
			1.65	3.0–3.6	I_{OH} = –24mA	2.2		
V_{OHB}	HIGH Level Output Voltage		1.65–1.95	3.0–3.6	I_{OH} = –100µA	V_{CCA} – 0.2		V
			1.65–1.95	3.0	I_{OH} = –6mA	1.25		
V_{OLA}	LOW Level Output Voltage		1.65–1.95	3.0–3.6	I_{OL} = 100µA		0.2	V
			1.65	3.0–3.6	I_{OL} = 24mA		0.55	
V_{OLB}	LOW Level Output Voltage		1.65–1.95	3.0–3.6	I_{OL} = 100µA		0.2	V
			1.65–1.95	3.0	I_{OL} = 6mA		0.3	
I_I	Input Leakage Current @ $\overline{OE}$, T/$\overline{R}$		1.65–1.95	3.0–3.6	0V ≤ V_I ≤ 3.6V		±5.0	µA
I_{OZ}	3-STATE Output Leakage		1.65–1.95	3.0–3.6	0V ≤ V_O ≤ 3.6V, $\overline{OE}$ = V_{CCB}, V_I = V_{IH} or V_{IL}		±10	µA
I_{OFF}	Power OFF Leakage Current		0	0	0 ≤ (V_I, V_O) ≤ 3.6V		10	µA
I_{CCA}/I_{CCB}	Quiescent Supply Current, per supply, V_{CCA}/V_{CCB}		1.65–1.95	3.0–3.6	A_n = V_{CCA} or GND, B_n, $\overline{OE}$, & T/$\overline{R}$ = V_{CCB} or GND		20	µA
			1.65–1.95	3.0–3.6	V_{CCA} ≤ A_n ≤ 3.6V, V_{CCB} ≤ B_n, $\overline{OE}$, T/$\overline{R}$ ≤ 3.6V		±20	µA
ΔI_{CC}	Increase in I_{CC} per Input, B_n, T/$\overline{R}$, $\overline{OE}$,		1.65–1.95	3.0–3.6	V_I = V_{CCB} – 0.6V		750	µA
	Increase in I_{CC} per Input, A_n		1.65–1.95	3.0–3.6	V_I = V_{CCA} – 0.6V		750	µA

DC Electrical Characteristics (2.3V < V_{CCB} ≤ 2.7V, 3.0V ≤ V_{CCA} ≤ 3.6V)

Symbol	Parameter		V_{CCB} (V)	V_{CCA} (V)	Conditions	Min.	Max.	Units
V_{IHA}	HIGH Level Input Voltage	A_n	2.3–2.7	3.0–3.6		2.0		V
V_{IHB}		B_n, T/$\overline{R}$, $\overline{OE}$	2.3–2.7	3.0–3.6		1.6		V
V_{ILA}	LOW Level Input Voltage	A_n	2.3–2.7	3.0–3.6			0.8	V
V_{ILB}		B_n, T/$\overline{R}$, $\overline{OE}$	2.3–2.7	3.0–3.6			0.7	V
V_{OHA}	HIGH Level Output Voltage		2.3–2.7	3.0–3.6	I_{OH} = –100µA	V_{CCA} – 0.2		V
			2.3	3.0–3.6	I_{OH} = –24mA	2.2		
V_{OHB}	HIGH Level Output Voltage		2.3–2.7	3.0–3.6	I_{OH} = –100µA	V_{CCB} – 0.2		V
			2.3–2.7	3.0	I_{OH} = –18mA	1.7		
V_{OLA}	LOW Level Output Voltage		2.3–2.7	3.0–3.6	I_{OL} = 100µA		0.2	V
			2.3	3.0–3.6	I_{OL} = 24mA		0.55	
V_{OLB}	LOW Level Output Voltage		2.3–2.7	3.0–3.6	I_{OL} = 100µA		0.2	V
			2.3–2.7	3.0	I_{OL} = 18mA		0.6	
I_I	Input Leakage Current @ $\overline{OE}$, T/$\overline{R}$		2.3–2.7	3.0–3.6	0V ≤ V_I ≤ 3.6V		±5.0	µA
I_{OZ}	3-STATE Output Leakage @ A_n		2.3–2.7	3.0–3.6	0V ≤ V_O ≤ 3.6V, $\overline{OE}$ = V_{CCA}, V_I = V_{IH} or V_{IL}		±10	µA
I_{OFF}	Power OFF Leakage Current		0	0	0 ≤ (V_I, V_O) ≤ 3.6V		10	µA
I_{CCA}/I_{CCB}	Quiescent Supply Current, per supply, V_{CCA}/V_{CCB}		2.3–2.7	3.0–3.6	A_n = V_{CCA} or GND, B_n, $\overline{OE}$, & T/$\overline{R}$ = V_{CCB} or GND		20	µA
			2.3–2.7	3.0–3.6	V_{CCA} ≤ A_n ≤ 3.6V, V_{CCB} ≤ B_n, $\overline{OE}$, T/$\overline{R}$ ≤ 3.6V		±20	µA
ΔI_{CC}	Increase in I_{CC} per Input, B_n, T/$\overline{R}$, $\overline{OE}$		2.3–2.7	3.0–3.6	V_I = V_{CCB} – 0.6V		750	µA
	Increase in I_{CC} per Input, A_n		2.3–2.7	3.0–3.6	V_I = V_{CCA} – 0.6V		750	µA

AC Electrical Characteristics

T_A = –40°C to +85°C, C_L =

Symbol	Parameter

Note:

7. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{osHL}) or LOW-to-HIGH (t_{osLH}).

Dynamic Switching Characteristics

Capacitance

Symbol	Parameter	Conditions	$T_A = +25°C$	Units
C_{IN}	Input Capacitance	$V_{CCB} = 2.5V$, $V_{CCA} = 3.3V$, $V_I = 0V$ or $V_{CCA/B}$	5	pF
$C_{I/O}$	Input/Output Capacitance	$V_{CCB} = 2.5V$, $V_{CCA} = 3.3V$, $V_I = 0V$ or $V_{CCA/B}$	6	pF
C_{PD}	Power Dissipation Capacitance	$V_{CCB} = 2.5V$, $V_{CCA} = 3.3V$, $V_I = 0V$ or $V_{CCA/B}$, f = 10MHz	20	pF

AC Loading and Waveforms

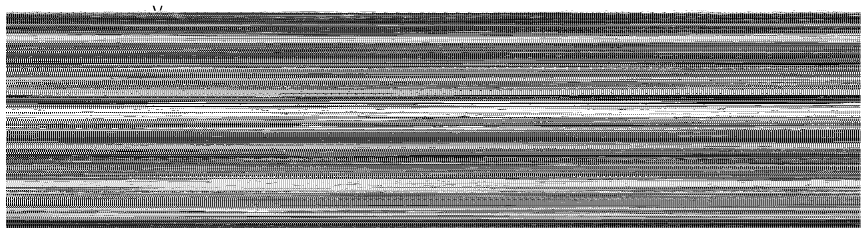


Figure 1. AC Test Circuit

Test	Switch
t_{PLH}, t_{PHL}	OPEN
t_{PZL}, t_{PLZ}	6V at $V_{CC} = 3.3 \pm 0.3V$; V_{CC} x 2 at $V_{CC} = 2.5 \pm 0.2V$; 1.8V ± 0.15V
t_{PZH}, t_{PHZ}	GND

Figure 2. Waveform for Inverting and Non-inverting Functions
$t_R = t_F \leq 2.0$ ns, 10% to 90%

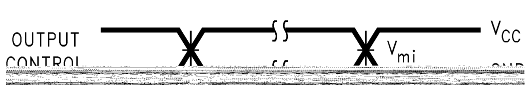


Figure 3. 3-STATE Output High Enable and Disable Times for Low Voltage Logic
$t_R = t_F \leq 2.0$ ns, 10% to 90%

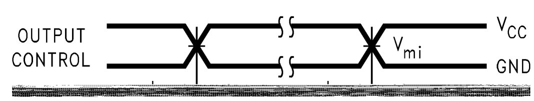


Figure 4. 3-STATE Output Low Enable and Disable Times for Low Voltage Logic
$t_R = t_F \leq 2.0$ ns, 10% to 90%

Symbol	V_{CC} 3.3V ± 0.3V	V_{CC} 2.5V ± 0.2V	V_{CC} 1.8V ± 0.15V
V_{mi}	1.5V	V_{CC} / 2	V_{CC} / 2
V_{mo}	1.5V	V_{CC} / 2	V_{CC} / 2
V_X	V_{OL} + 0.3V	V_{OL} + 0.15V	V_{OL} + 0.15V
V_Y	V_{OH} – 0.3V	V_{OH} – 0.15V	V_{OH} – 0.15V

Physical Dimensions

Dimensions are in millimeters unless otherwise noted.

Physical Dimensions (Continued)

Dimensions are in millimeters unless otherwise noted.

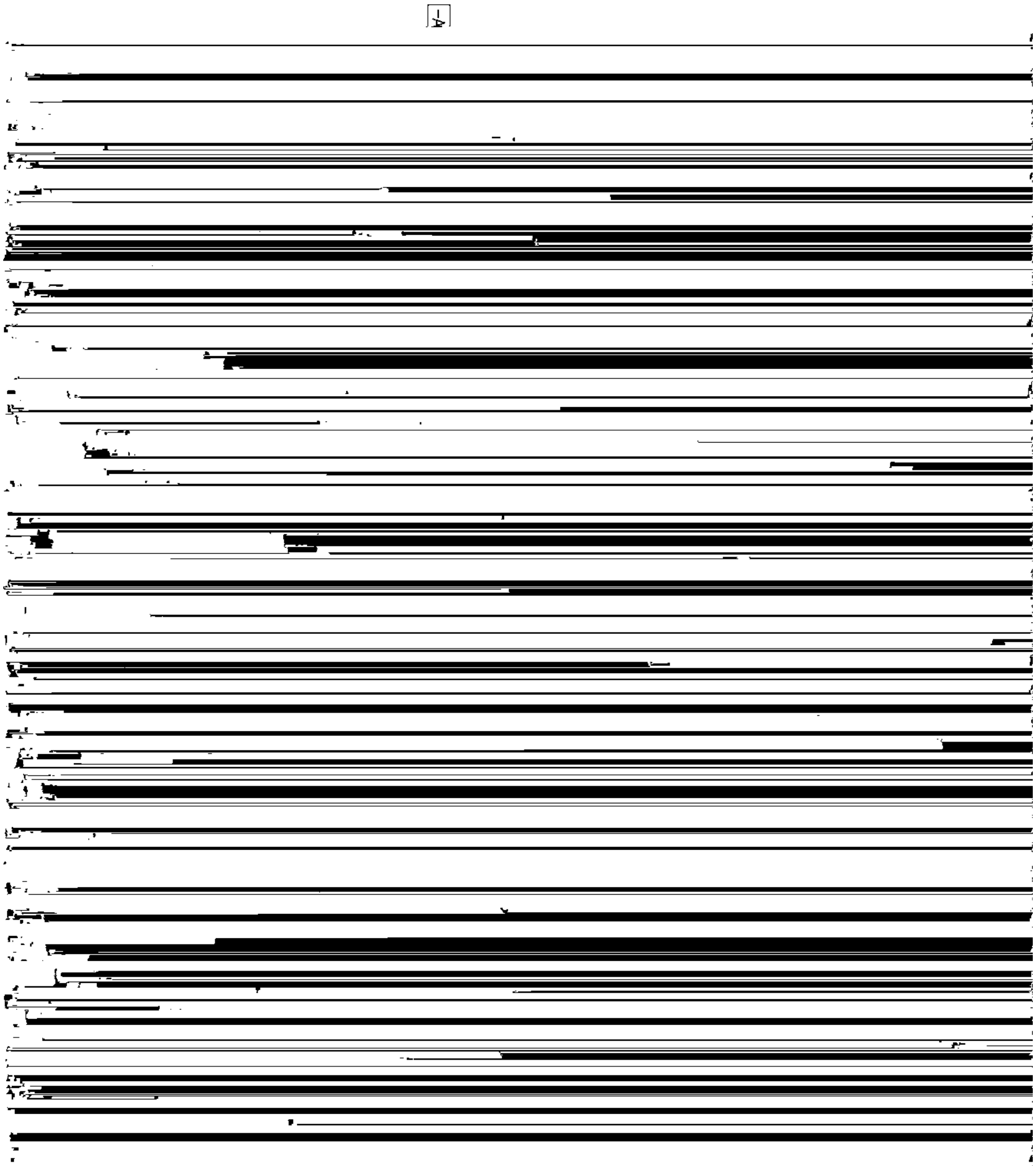


Figure 6. 48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD48

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Datasheet Identification	Product Status	Definition
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