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74LVX273
Low Voltage Octal D-Type Flip-Flop

General Description

The LVX273 has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset ($\overline{MR}$) input load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output.

All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the $\overline{MR}$ input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements. The inputs tolerate up to 7V allowing interface of 5V systems to 3V systems.

Pb-Free package per JEDEC J-STD-020B

Features

■ Input voltage translation from 5V to 3V

Logic Symbols

IEEE/IEC

Connection Diagram

Truth Table

Pin Descriptions

H = HIGH Voltage Level
L

X = Immaterial

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Logic Diagram

AC Electrical Characteristics

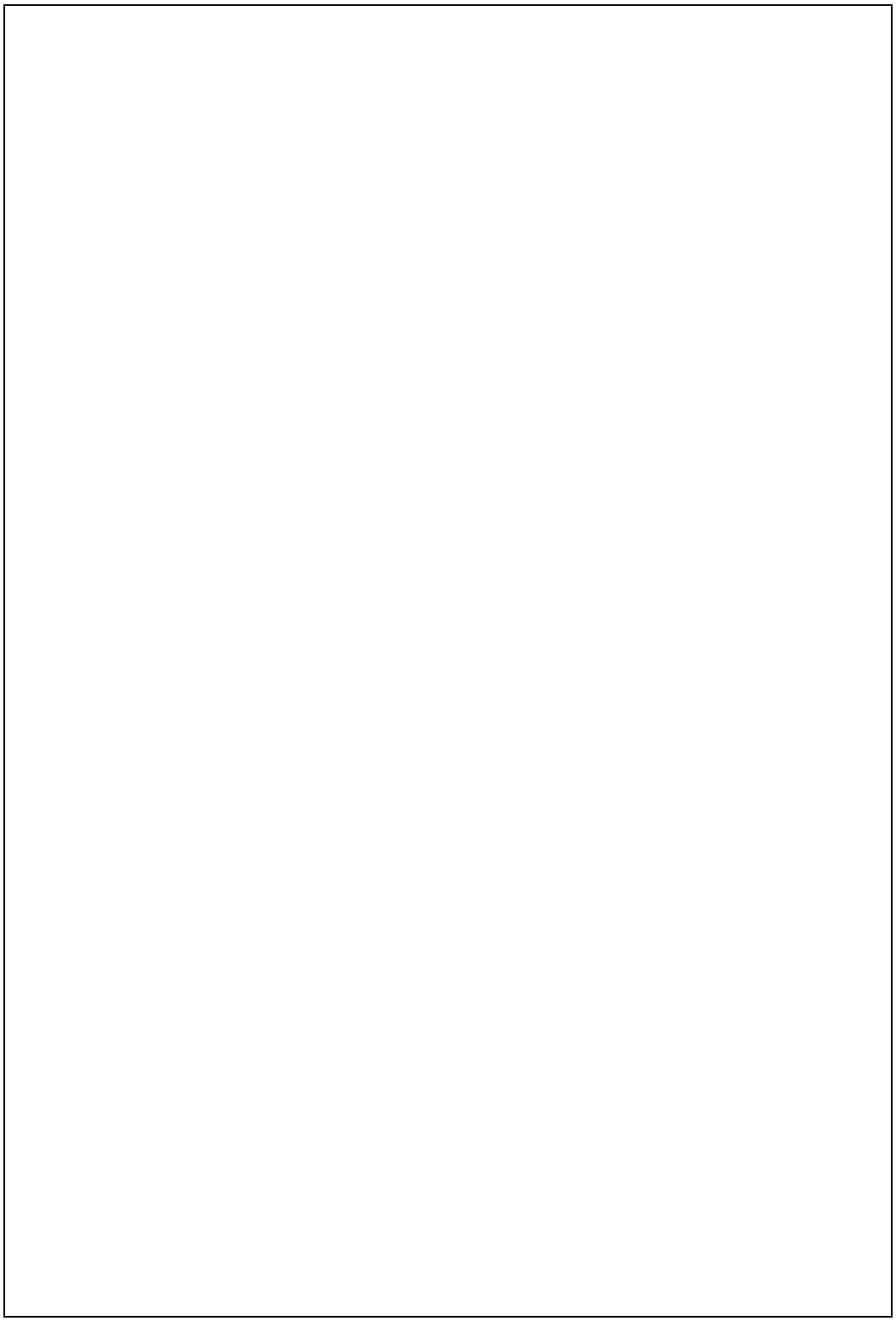
Symbol	Parameter	V_{CC} (V)	$T_A = +25°C$			$T_A = -40°C$ to $+85°C$		Units	C_L (pF)
			Min	Typ	Max	Min	Max		
t_{PLH}	Propagation	24 Tc [(a1 Tf 0.4 0 TD (C)Tj 2.135[25.46n(o)-0.344u68 TD 0 Tc (t)Tj 851[[5.(W0314u)19.1(ati)5.15 c)-11.3(a)0.2(lc)-11.3(u)-22(l)-0 0 83(u							

Note 4: Parameter guaranteed by design. $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$

Capacitance

Note 5: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Physical Dimensions



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